Enhanced Floor plan Algorithm for Ultra Complex SoC's

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Abstract

With the increase in the functionalities, complexity and instance count of the designs, floor planning has become a most critical task which needs lot of manual effort, time and machine usage. As the technology of shrinking, there are analog circuits which are dominating the chips; there are lot of floor plan rules which is mandatory and need to be done manually and it takes time, energy and manpower which is being costly. We are developing the algorithm of enhanced automatic floor plan by honoring all the floor plan rules and allowing the power and area optimizations.

Keywords: Physical design (PD), Enhanced Floor plan algorithm, Macro placement.

1. Introduction

Physical design (PD) is the process of transforming the logic design into layout representation. The physically represented design has to meet the functional and performance requirements. Performance requirements are in terms of Area, Power and Frequency of operation [1]. Signal Integrity became the major cause of design failure due to continuous shrink in layout dimensions and the complexity of the design. Sub threshold leakage contributes to large amount of power dissipation of the chip, which is uncontrollable for these lower technologies.

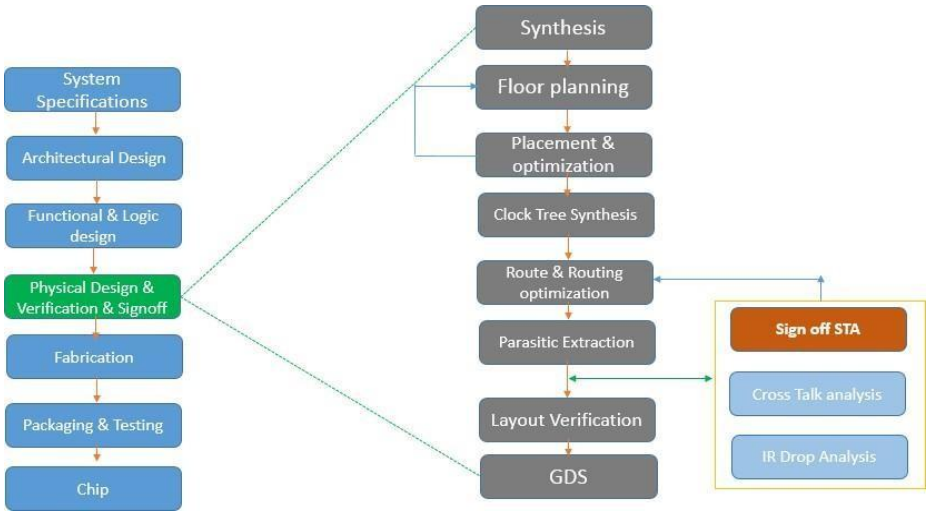

Figure 1 Standard Physical Design Flow for a typical ASIC

Now major part of the chip's power is coming from its leakage power, which is becoming important with advanced technologies. In order the drawn or implementing designs to meet geometric, timing and power constraints Physical Design (PD) automation has comes into existence to carry out such designs using electronic aided automation tools.

2. Floor Plan

This is the first major and important step to implement a design physically. Quality of the chip is decided by the efficiency of floor plan. Here, defining block or chip size, allocation of routing resources for power, macro placing and reservation of space for standard cells will be done. The quality of floor plan decides the efficient of next stage sin the implementation like placement, routing and timing closure [3].

2.1 Floor plan Steps

1. Import technology files library files
2. Import Net list &Design Constrains
3. Determine ASIC and Core sizes
4. Create I/O pads sites and standard cell rows
5. Create Power and ground rings
6. Macro placement
7. Create Macro placement and ground rings
8. Floor plan refinement

2.2 Floor plan Inputs of IP Core

This includes providing different inputs required to complete the floor plan. They are technology information; libraries, synthesized design netlist, and Design constraints [2]. Technology information is provided in the form of tech file,which contains data such as Manufacturing Grid, Routing grid, Standard cell placement tile, Routing layer definition, Placement and routing blockage layer definition, via definition, Conducting layer density rule, Metal layer slotting rule, Routing layer physical profile etc.

Technology Libraries: They are same as those used for synthesis but in a different format i.e. NDM (New Data Model).

Design Net list: After successful synthesis process net list been obtained. The output of synthesis is the starting material for Physical Design.

Design Constraints: This can also be obtained from synthesis outputs as constraints been already defined during synthesis process. Some PD related constraints can also be added to the same file.

2.3 Floor plan Setup

Site Array and Site row definitions has to be provided to the tool. Site Array is a specific area which contain site rows of same height. Site rows are places where standard cells will be placed. Modular Grid and Track Patterns has to be defined in design area. Modular Grid is primary thing to be considered because this will helps to integrate all the blocks of the design. Track Pattern is also dependent on modular grid of the technology. This defines the number of tracks can supported in specified area, and each track's pitch, width will be defined. Both are technology dependent data. Routing Metal Layer definition has to be done. Where each metal layer width and alignment (direction) to be specified. Along with layer definition extraction related information about this layer has to be provided. This also technology related information and provided in TLUPLUS files format.

2.4 Floor plan Procedure

Floor plan Process will begin by creating boundary of the design. For the block under implementation design height and width are provided in DEF file. Any placement and/or routing blockages that are specific to technology or design, has to be created [4]. One of such blockage is boundary blockage to avoid cell placement to be done very near to boundary.IO placement should happen from the data available in DEF file. Where all pin placement information is provided. Information includes pin location, metal layer on which pin has to be built and IO pad dimensions. And then create IO pad blockage region to avoid cell placement in IO region. Up on various trials of complete PnR process, for the design considered DEF (Design Exchange Format) file been created. Which contain optimum IO and area information.

Site array and site row creation: For the obtained Technology three type of standard cells are available. Core, Core2h and bonus core. Core and Core2h are of same height but of different widths, so one site array will be sufficient for both of them. Whereas bonus core cells of double height cells so site array has to be defined separately for these cells.

3. Placement

During floor plan creation of core area, placement of macros and structure of power network is done. After doing the mentioned task during floor plan, for tool to place standard cell it is the right time. Determining the location of each standard cell (or component) on the die is major objective of placement stage. While doing so various factors like timing specifications of the design, length of interconnections and power dissipation will come into existence [6]. As geometries are decreasing continuously Interconnect length determines the performance of the design, which is majorly decided by placement solution. Also routability is also decided by placement quality only. Placement not only places the standard cells from the net list but also optimizes the design, to avoid any timing violations in the design.During placement, all standard cells of the design are located within the design area. Placing and selecting these standard cells is determined from area, timing and power constraints [5]. Placement also determines the utilization of the block, where utilization factor is defined as the ratio of gate and routing areas to the total area of the block.

3.1 Placement Setup

The wire load models will be used at pre-placement stage. These wire load models should be removed before the placement starts. As these placement uses the RC values from the extraction possibilities in the setup. Clock reconvergence pessimism removal (CRPR): the clock trees need to share as many buffers as possible in order to reduce the OCV effects. The timing calculations will be shared by the clock path that is the common clock paths will have same delays so that can be reduced. The delays through common cells cannot be different as when they are calculated as launch path and the capture path. The difference between the earliest arrival time and the latest arrival time is known as Clock reconvergence pessimism (CRP). The CRP will be added to capture path for setup timing in pessimism removal. For hold timing the CRP will be subtracted from capture path.

During data path optimization, Buffer area utilization should be defined. TIE cells are used to power the standard cells these will be placed along with the standard cells. Maximum fan out should be given to TIE cells. The tie-high and tie-low cells will be connected to power and ground. But in lower level technologies there may be ground bounce or power bounce if the gate is connected to power or ground of the transistor. These cells will be present in the standard cell library[7]. The leakage optimization options will also be given at placement stage. The library contains four type of cells they are Vt cells, high Vt cells, standard Vt, nominal Vt, Ultra low Vt. Ultralow Vt cells are not used to provide more flexible for optimization at later stages. Maximum density of cells should be placed in design area if place coarse maximum density is defined. Specify cell spacing: For some specific cells, there are settings based on

physical DRC's. And also should be given with DFM spacing rules: larger vias will be placed to improve the yield. So that the failure of vias will gradually reduce in the design.

4. Existing Design

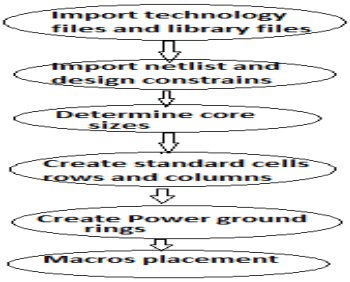

Figure 2 Exiting design flow chat

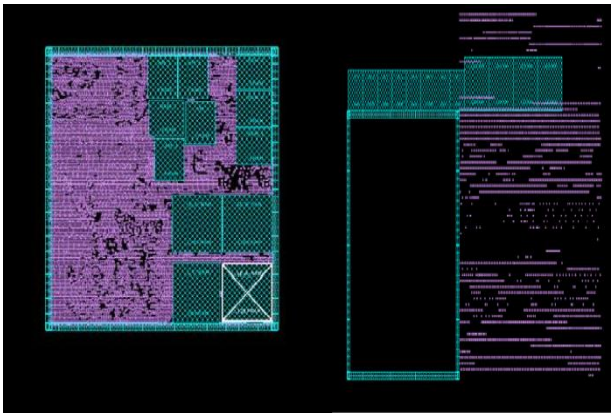

Figure 3 macros placement

Normally macros placing with the mouse, when the count of the macros is less then50 no-problem but its count is more than 100 then it will take more time to go for the next stage. (Placement, cts,routing).And generally, we are placing the macros randomly in the core area[8]. Due to this random arrangement of the macros, we cannot use core area effectively, and addition to this, usage of Metal layers also increases, Conjuction also increases. So it took more time to go for the next stage (placement, cts, routing).

To eliminate these disadvantages we are moving towards the automatic floor plan algorithm. It applied to all shapes (square shape, rectangle shape, rectilinear shape).

The runtime experiment considerations is shown below

. Default: 1hrs 30min

Experiment: 1hrs 20min

The congestion number of the experiment is shown below.

Default: 0.22% H + 0.23% V

Experiment: 0.19% H + 0.22% V.

5. Proposed Design

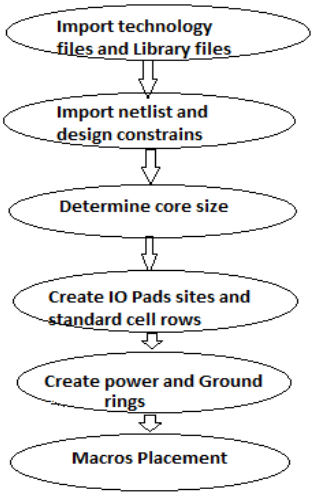

Figure 4 Proposed Design flow chart

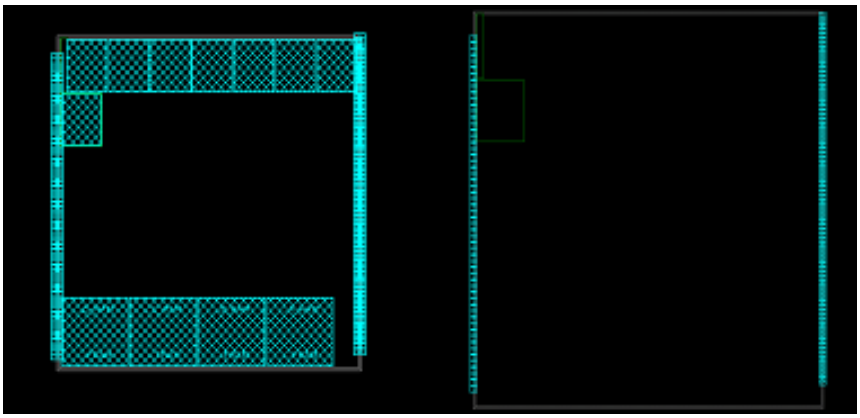

Figure 5 Macros and I/O pins plasing

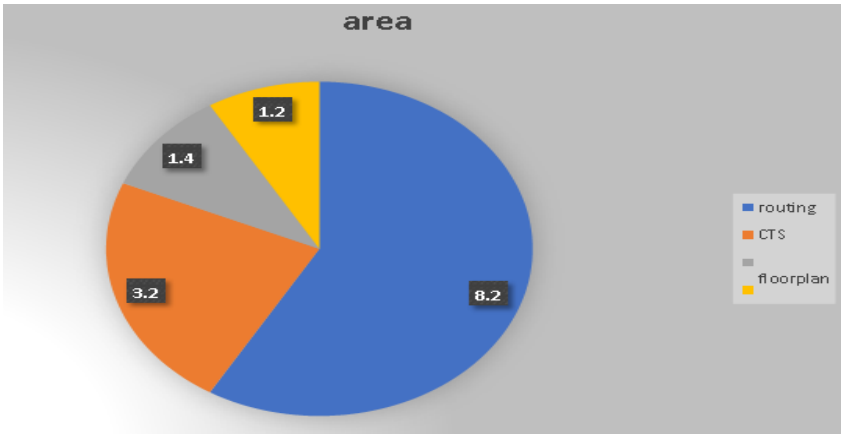

Figure 6 core utilization at each stage

With the help of automatic floor plan algorithm,(which as shown above) we place the Macros and I/O pads in correct manner which has shown above figure 5. so that we can use the core area and usages of metal layers effectively . Due to this congestion reduced, we can go to the next stage quickly. In the above figure 6 shows core utilization at each stage that means for routing pulpous use more core area due to that from one stage to another stage going taken time very less[9]. After proper floor plan completion results to be verified are check report and utilization report. Figure 7 shows check report of the design and Table 1 shows the corresponding utilization results of implementing design [10].

The runtimes of the experiment is shown below

. Default: 1hrs 30min

Experiment: 1hrs

The congestion number of the experiment is shown below.

Default: 0.22% H + 0.23% V

Experiment: 0.10% H + 0.15% V.

Utilization Report	**Automatic floor plan**	**Manual floor plan**
Utilization Ratio	0.4536nm^2	0.6536nm^2
Total Area	105753.6nm^2	105753.6nm^2
Total Capacity Area	105525nm^2	105525nm^2
Total Area of macros	47864.26nm^2	48064.26nm^2
Area of hard blockages	634.1691nm^2	834.1691nm^2

Table 1.Utilization Report

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-----------------------------------------
Number of Written DEF Constructs
-----------------------------------------
VERSION                                  :  1
DIVIDERCHAR                              :  1
BUSBITCHARS                              :  1
DESIGN                                   :  1
UNITS                                    :  1
DIEAREA                                  :  1
ROW                                      :  2999
TRACKS                                   :  274
COMPONENTS                               :  437596
PINS                                     :  3679
BLOCKAGES                                :  28
SPECIALNETS                              :  2
NETS                                     :  431617
```

Figure 7 Floor plan Check Report of the Design

6. Conclusion

In this paper, applied enhanced automatic floor plan algorithm was reduced the power and area compared to existing deign of standard cell approach. The utilization report shows the comparison of automatic and manual floor design. In quality IC implementation floor-planning is the foundation. The decisions made regarding I/O pad placement, macro placement, partitioning, pin assignment, power planning that ripple through the PNR flow. To handle extremely large data sets, design variability and complexity designing need this algorithm which enable's fast and high-quality floor-planning.

7. References

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