

# Design and Implementation of Efficient 8-Bit SIPO Shift Register

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**Abstract:** Area and power are main design constraints in analog and digital circuits. In this paper, a low-power 8-bit shift register is implemented by using true phase single clock (TSPC) D- flip flop which is based on single clock and two clocked transistors. The proposed design successfully solves the long discharge path problem which is bound to occur in conventional type of D-Flip Flop. This paper describes 8 bit serial in parallel out (SIPO) shift register using True Single-Phase Clock(TSPC) technique which reduces an area in terms of transistor count by 85.29%.

**Keywords:** Reversible Logic, Area, Power, Sequential Circuits.

## 1. INTRODUCTION

First shift register is built using vacuum tubes [1]. Thereby they started to minimize the area and power consumption. Today area utilization, power dissipation [2-4] becomes an important design issue in VLSI circuits. This tends to pay attention on power dissipation and number of transistors. When it comes to portability of devices, power dissipation is an unavoidable constraint [5-8]. Due to scaling of technologies, the power consumption per unit area of the chip has risen tremendously.

The main contribution of this work is to implement 8 bit SIPO shift register using True Single-Phase Clock technique. Area and power aware design is described in this paper. The schematic entry and functional verification is successfully done using DSCH tool.

Rest of the paper is arranged as follow: Section 1 highlights an introduction part. Section 2 demonstrates the existing types of shift registers. Section 3 focuses on the proposed approach. Section 4 demonstrates experimental results and section 5 concludes the paper.

## 2. Shift Registers

Sequential has two states. It maintains the state until receiving a trigger. Figure 1 shows the general block diagram of sequential circuits. Output depends on the present input and past outputs [9-10]. There is a memory unit to store immediate results.

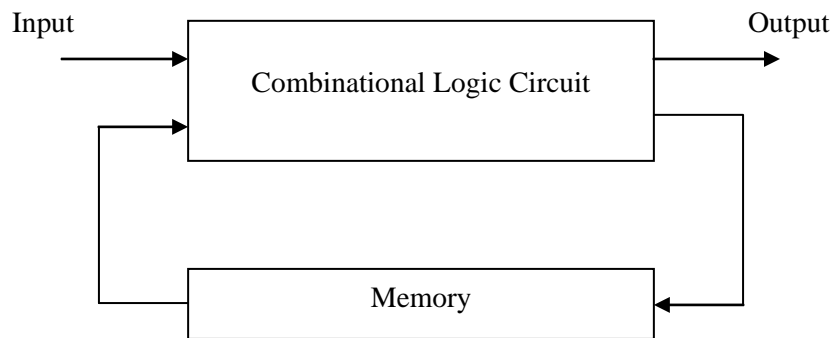


Figure 1. Generic Architecture of Sequential block

Types of Shift registers (SR) are as shown in Figure 2.

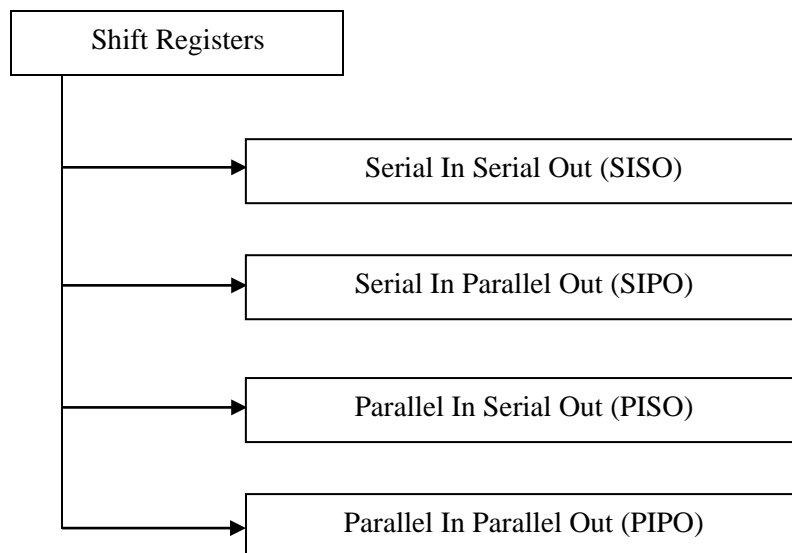


Figure 2. Types of SR

### Serial In Serial Out Register:

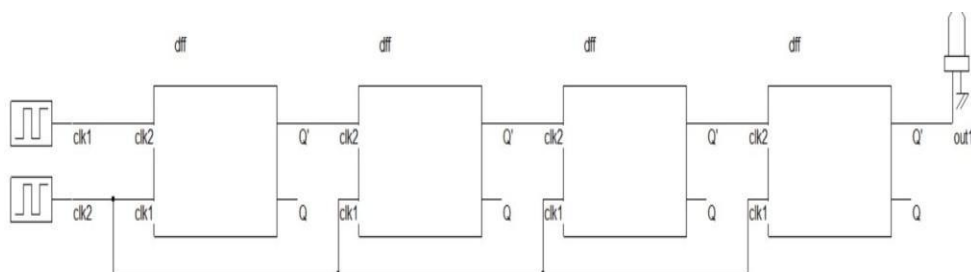


Figure 3. Typical Architecture of SISO Block

### Serial In Parallel Out Shift Register:

It consists of serial input and gives a parallel output,[11-12]. Figure 3 shows the block diagram of SIPO register. A conventional block requires 4 D flip flops to implement 4-bit SIPO register.

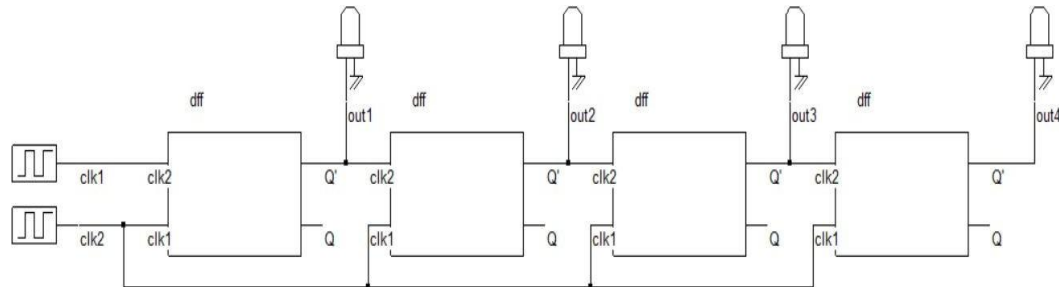


Figure 4. Typical Architecture of SIPO Block

### Parallel In Serial Out Shift Register:

This block can be implemented with four D-flip-flops, where the CLK signal is connected simultaneously to all the FFs [13-14].

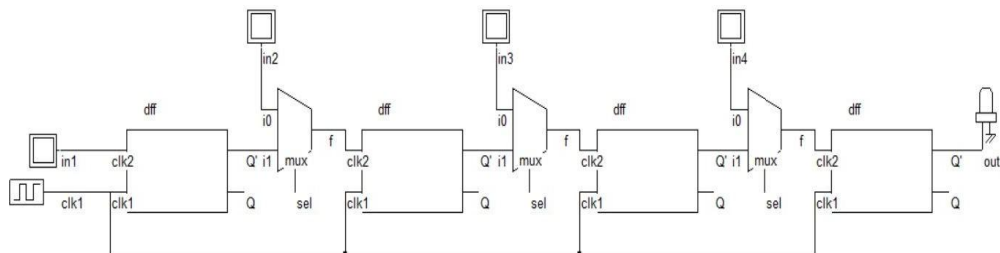


Figure 5. Typical Architecture of PISO Block

### Parallel In Parallel Out Shift Register:

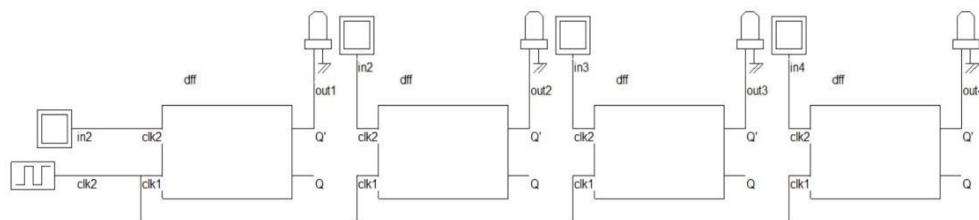


Figure 6. Typical Architecture of PIPO Block

Here the data is given as input individually for every flip-flop [15], as well as the output is also received separately from every flip flop.

### 3. Proposed Research Method

In this paper, two techniques are implemented.

#### D Flip flop implemented with Latches using NAND Gates

Four NAND gates are required to implement D Latch and with cascading two latches, one Flip flop is implemented as shown in Figure 8.

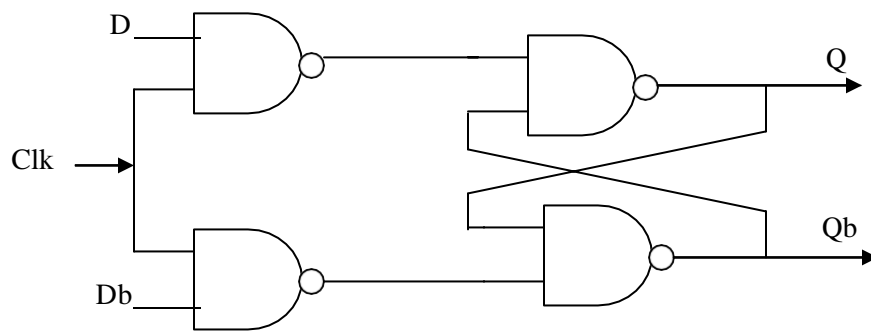


Figure 7. Simple Latch

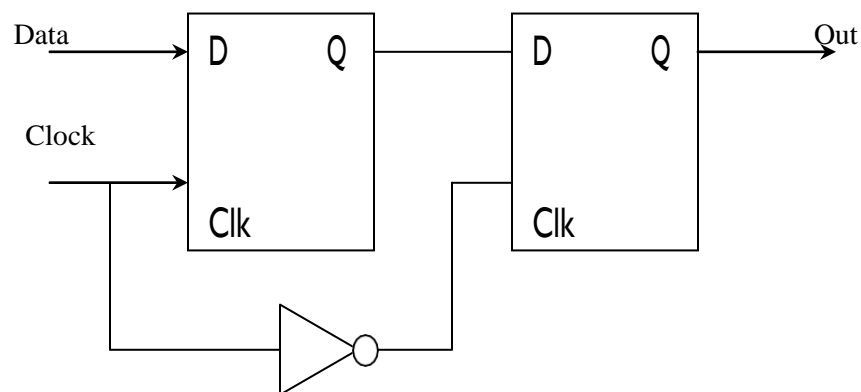


Figure 8. D Flip Flop

#### D Flip Flop implemented using True Single Phase Clock Latch (TSPC):

This circuit consists of seven transistors out of which two inverters are present. Schematic of latch is as shown in figure 9.

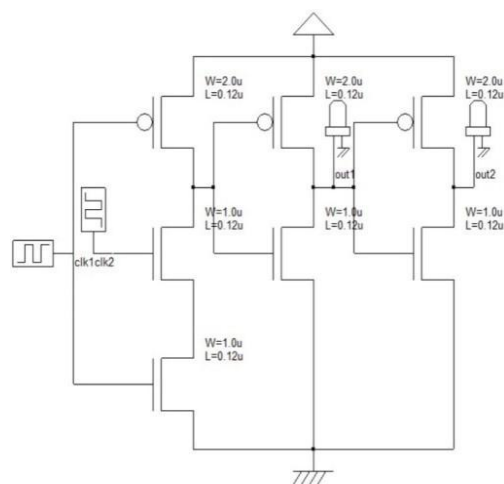


Figure 9. Schematic of TSPC Latch

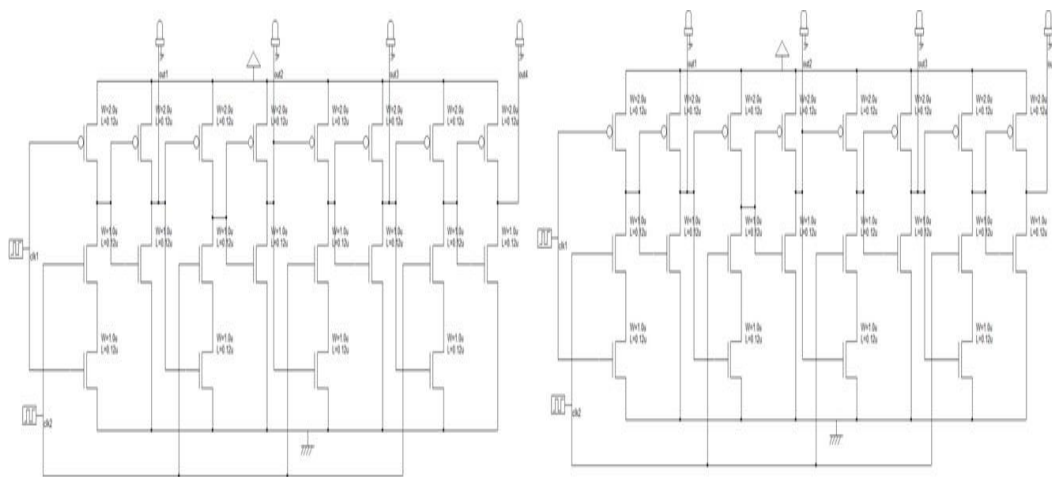


Figure 10. Schematic of 8-bit SIPO Shift Register

#### 4. Experimental Results and Discussion

All the schematics are functionally verified by their truth tables. These waveforms are the simulation results of circuits, which are designed using electronic design automation DSCH tool. From the Table 2, it clearly shows that conventional method requires 272 transistors where as TSPC based approach required only 40 transistors. Therefore, reduction in transistor count demonstrates area optimization.

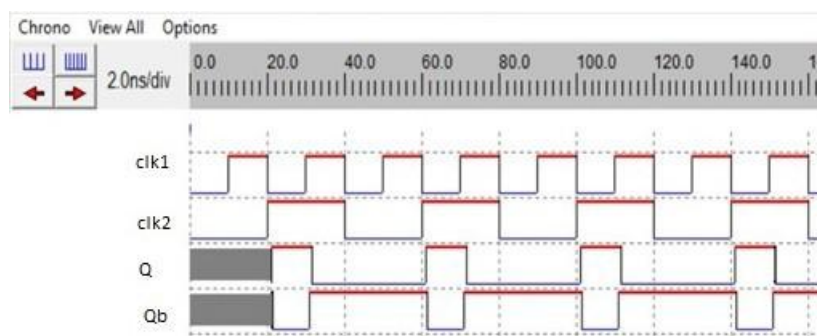


Figure 11. Timing waveforms of D-FF circuit

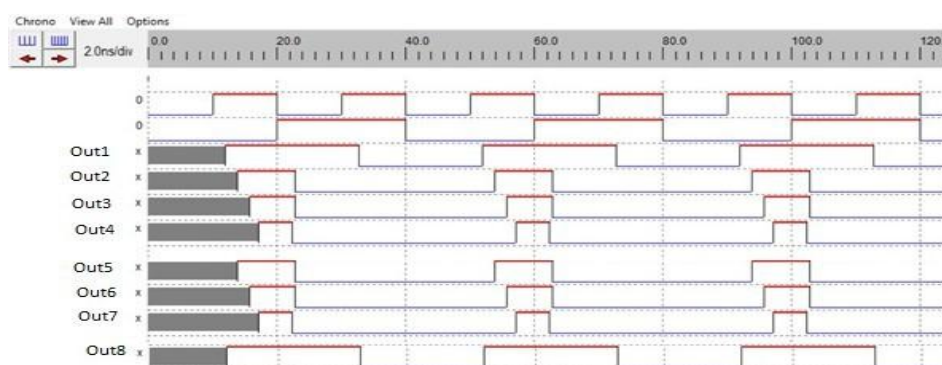


Figure 12. Timing waveforms of 8-bit SIPO Shift Register

Table 1: Power consumption and Area

8-bit SIPO shift register	Power consumption ( $\mu\text{W}$ )
Conventional method (NAND LATCH)	493.62
Proposed method (TSPC LATCH)	117.66

Table 2: Area (in terms of transistor count) Comparison

Techniques	8-bit SIPO shift register
Conventional method (NAND LATCH)	272
Proposed method (TSPC LATCH)	40

## 5. Conclusion

In this paper, low area and power efficient 8-bit serial input parallel output shift register is designed using TSPC D-FF. The properties are improved by reducing the number of transistor and minimizing the discharging path. The circuit is also very simplified unlike the convention NAND latch based SIPO. In this paper, two latch systems are described namely 1) NAND latch 2) TSPC latch. By implementing and comparing these two methods, we conclude that by enhancing and implementing good latch system, we can control area and power consumption. The conventional method which uses the NAND latch for circuit implementation requires more number of

transistor's than TSPC latch based SIPO. In NAND latch, each latch requires 4 transistors. Every D-FF requires 2 latches and one inverter which has total number of transistor count as 34. This means the fully functional 8-bit SIPO is required 272 transistors. In TSPC latch based D-FF requires only 7 transistors but as the SIPO don't require Q' output therefore it can reduced to 5 transistors and the SIPO block requires only 40 transistors. It reduces an area by 85.29 %.

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