A Reconfigurable Variable Resolution Digital Architecture for Diverse Analog to Digital Converters

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Abstract: *The bottlenecking role of Analog to Digital Converters (ADCs), while using it in variety of applications, is well known to the designer since past. This stimulates to have a universal ADC architecture which can satisfy needs of diversified applications.*

The work presented in this paper is based on this thought and successfully demonstrates, 'Xilinx Spartan 3E' FPGA based, hardware realization of a Reconfigurable Digital Section Architecture that can be configured for Multiple iterative type of Analog to Digital Converters (ADCs). This single reconfigurable architecture has provided compatibility to interface with analog sections of three different architectures i.e. Successive Approximation ADC or Single Stage Pipeline ADC with feedback or Dual Slope ADC and empowers variable resolution up to 8 bits. This facilitates flexibility in application specific selection of suitable ADC architecture and thus increases diverse application areas at the cost of design complexity.

The architecture utilizes 2.5 % of total gate count and 27% input output blocks of FPGA while operating at 30 MHz clock frequency. The on-chip power consumption is 54.93 mW. The results show reduction in effective power utilization, pin count and clock skew without scarifying operating speed as compared to single time multiplexed Digital architecture for these ADCs, synthesized on the same FPGA.

Keywords: **ADC, SAR, FPGA, FSM, CU, GDPU, SoC**

1. INTRODUCTION

Today's scenario is largely focusing on integrating number of sectors through automation. Soft automation systems and hard automation systems are dominating the world. In hard automation systems, embedded system is an obvious choice. Design parameters of embedded systems mainly puts constraints on size, power consumption and speed of operations. Most of the embedded systems essentially employ Analog to digital converters to facilitate interface between analog signal and digital circuits but comprises single on chip ADC architecture. Single ADC architecture always limits the application range of SoCs, majorly due to limitations on resolution and speed of the ADC [1]. Various standard as well as reconfigurable and variable resolution ADC architectures are presented by researchers with different operating principles [2], [3], [4]. Some of them were implemented with reconfiguration of analog devices or insertion of additional devices/components for modifying the existing architectures. Variable resolution is needed in various domains like wireless networks and helps to keep the low data rate as required. Successive approximation ADCs and Pipeline ADCs are useful for high-speed applications [5]. Integrating type ADCs, such as Dual Slope ADC, are useful for applications those required high resolution with minimum effect of noise and temperature.

SAR ADC is employed on many MCUs due to its comparable versatility in speed and performance [6]. Resolution of ADC made adaptive to the nature of input signal for different applications [7]. One of the attempts is to design reconfigurable ADC for medical applications with variable resolution capability where tradeoff between power and accuracy is demonstrated [8]. Architectural modifications are done to achieve different resolutions at different sampling frequency [9]. Reconfigurable ADCs are designed to aim at reduction in the comparator requirements pertaining to signal bandwidth and system sampling rate [10]. FPGA based ADC designs are suitable to alter themselves by changing firmware according to applications [11]. This motivates us to design and develop an ADC architecture with variable resolution that can fulfill diverse requirements of SoCs. The work presented in this paper is concerned with design of single digital output stage architecture that can be reconfigured for one of three different types of analog-to-digital converter architectures but one at a time.

Section II presents design method used for this Reconfigurable architecture with its design requirements and considerations. It illustrates block wise system design and related methods used for this work. Section III emphasizes on simulation results of individual block sets of the architecture and whole system architecture. Section IV concludes the work in summarized format.

2. DESIGN OF RECONFIGURABLE SINGLE DIGITAL SECTION ARCHITECTURE FOR MULTIPLE ANALOG TO DIGITAL CONVERTERS

Block diagram of the overall system with analog section and the digitally designed system has been shown in figure 1. The design of analog section is not part of this work. The format of an 8-bit instruction is depicted in figure 2. The architecture accepts input from output of external comparator and eight-bit instruction from SoC for configuring architecture for specific type of ADC. The architecture comprises Control Unit (CU) and Generic Data Path Unit (GDPU). CU issues various control signals to GDPU and to external data path units of the architecture. GDPU works as an eight-bit parallel load register in SAR mode, an eight-bit counter in Dual Slope mode and shift register in case of Pipeline mode.

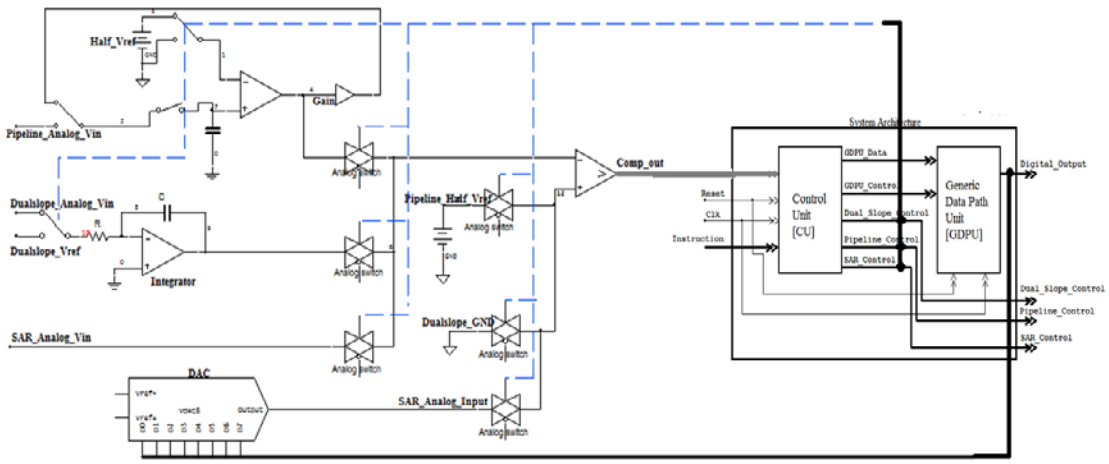


Figure 1. System Architecture of the Design

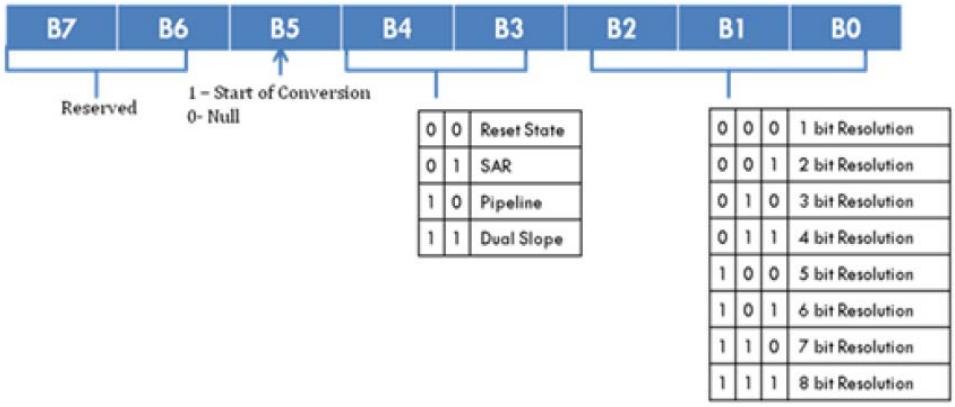


Figure 2. Eight Bit Instruction

As shown in figure 2, bits B2-B0 of the instruction define resolution in the range from one (1) bit to eight (8) bit, bits B3-B4 defines specific ADC configuration and thus facilitates user-based architecture. GDPU processes the data to provide output bits. In the instruction, 'Bit B5' is Start of Conversion (SoC) bit and Bits 6-7 are reserved for addition of future features.

Figure 3. depicts block diagram of CU which operates on 'clk' and 'reset' signals. This microarchitecture unit is designed and implemented using FSM technique and consists of instruction decoding logic, control signal generation logic and variable resolution control logic. 'Instruction decoding logic' decodes an instruction received from SoC. 'Control signal generator', generates control signal for GDPU and external units to configure the architecture. Resolution control logic limits digital output as programmed through instruction.

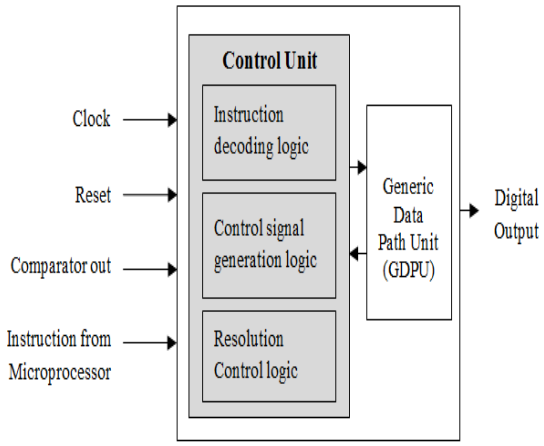


Figure 3.a Control Unit (CU)

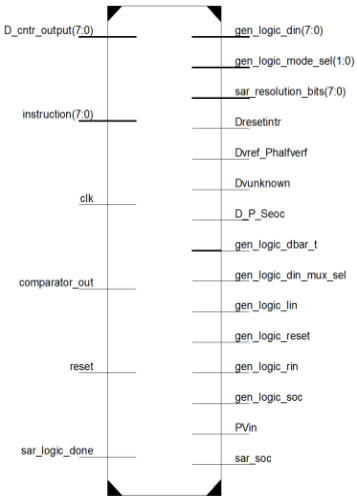


Figure 3.b Schematic of Control Unit (CU)

RTL schematic of control unit is shown in Figure 3.b which accepts external comparator's data output (comparator_out) as an input or eight-bit output from dual slope counter (D_cntr_output) or overflow signal from SAR logic (sar_logic_done). 'D_P_Seoc' signal of CU indicates completion of conversion.

Generic Data Path Unit (GDPU) is data processing unit that generates maximum eight-bit digital output. Figure 4 depicts schematic design of GDPU.

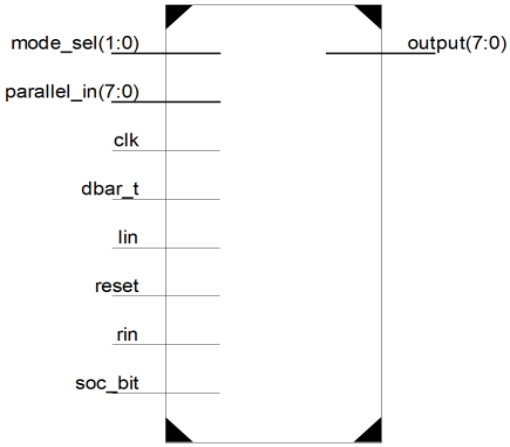


Figure 4 Schematic Design of General Data Path Unit (GDPU)

GDPU designed as structural unit, generates digital output according to the architecture configured. It comprises eight flip-flops with each having 4:1 multiplexer to select one of the GDPU inputs from 'parallel_in', 'lin', 'rin', according to configured architecture. It operates as a clock synchronous data path unit and being reset either with master reset or the reset signal generated by CU.

Different operational modes of GDPU are shown in table 1. Mode selection is done through 'mode_sel input' provided by CU. GDPU input signals are governed by CU. 'soc_bit' received from CU indicates start of conversion operation. Eight bit 'parallel_ in' input is parallel data input, provided by CU in register mode operation.

Table 1. CU, GDPU inputs and operating modes

Input	SAR Mode	Pipeline Mode	Dual Slope Mode
Instruction (B4:B3)	01	10	11
Operating mode	Shift Register (PIPO)	Shift Register (SIPO)	Counter
Mode_sel(1:0)	00- Parallel in parallel out 01- Retain output	10- Eight bit left shift 01- Retain output	01- Retain output 00- Parallel in parallel out
Parallel_in (7:0)	From SAR logic	NA	NA
Dbar_t	0	0	1
lin	NA	NA	NA
rin	NA	From Comparator	NA
SoC_bit	Asserted by CU	Asserted by CU	Asserted by CU

3. RECONFIGURABLE DIGITAL ARCHITECTURE: DESIGN FLOWCHART

Figure 5 shows flow chart of logic design of Reconfigurable Digital Architecture. It employs asynchronous, hardwired reset or power on reset to reset the configured architecture. Figure 5a. shows behaviour of CU after application of eight-bit instruction along with clock and comparator output.

Control signals are generated according to configured architecture and resolution. Figure 5b. depicts timing simulation results for SAR digital architecture. In SAR configuration, GDPU works as PIPO mode register and accepts input from SAR logic.

Figure 5c. depicts timing simulation results for pipeline digital architecture. In this configuration GDPU works as right in left out SISO mode shift register.

Figure 5d. shows timing simulation of dual slope digital architecture in which GDPU works as a four bit binary counter.

The functioning of each configuration is validated separately through separate test vectors.

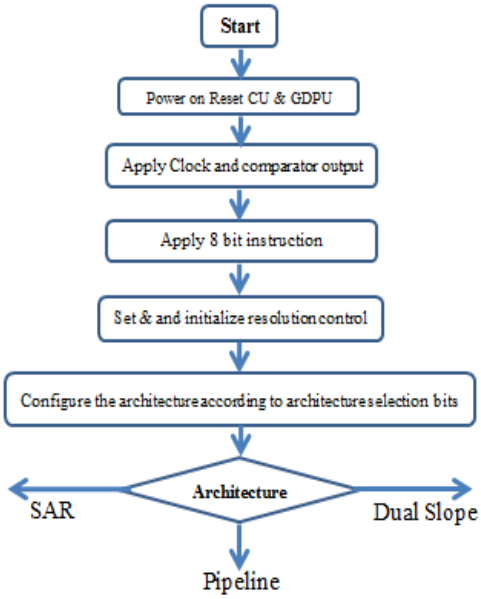


Figure 5 CU at Power on Reset

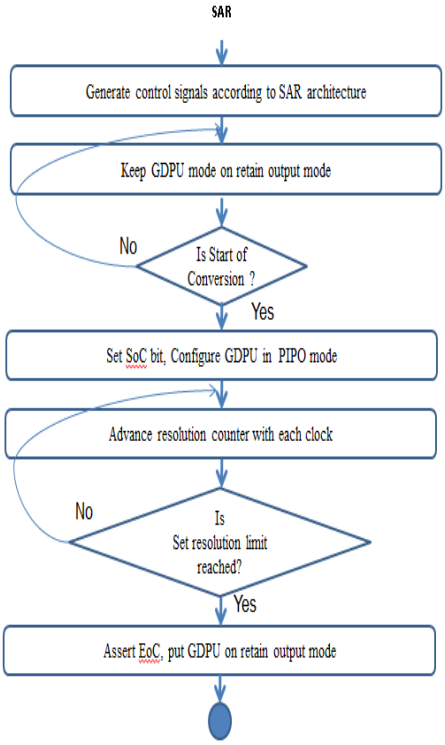
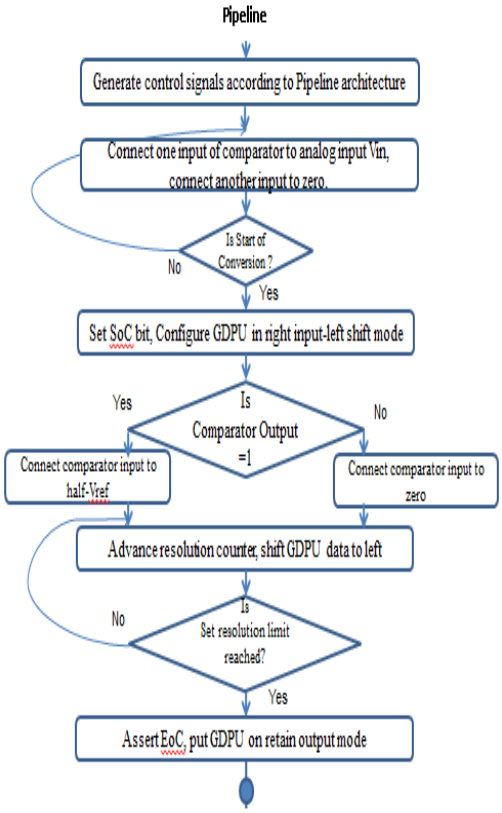


Figure 5 b. SAR architecture



. Figure 5 c. Pipeline architecture

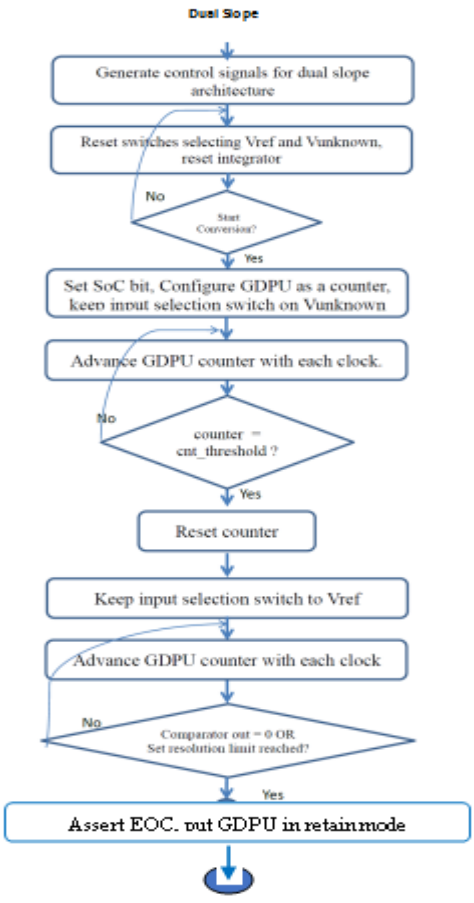


Figure 5 d. Dual slope architecture

4. RESULTS

Results are verified by applying test vectors. Test bench stimulates the architecture to test functionality of digital RC ADC architecture for variable resolutions of SAR, Dual slope and Pipeline ADC configurations.

[A] SAR Architecture:

Figure 6 depicts waveforms for the configuration of 8 bit SAR Architecture with the Start of Conversion signal ('sig_gen_soc'). Comparative output is 1 for second,sixth, seventh and eighth clock cycles. Accordingly output changed from MSB to LSB in SAR. At eighth clock cycle, eoc signal is asserted. It indicates end of conversion.

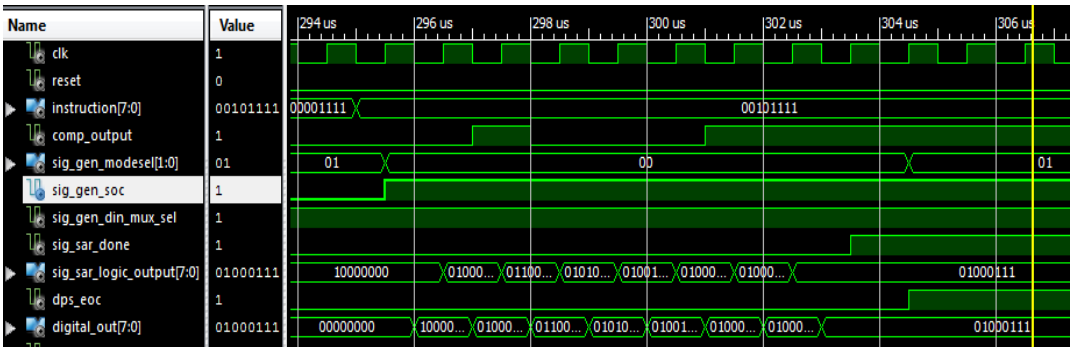


Figure 6. SAR 4 bit resolution

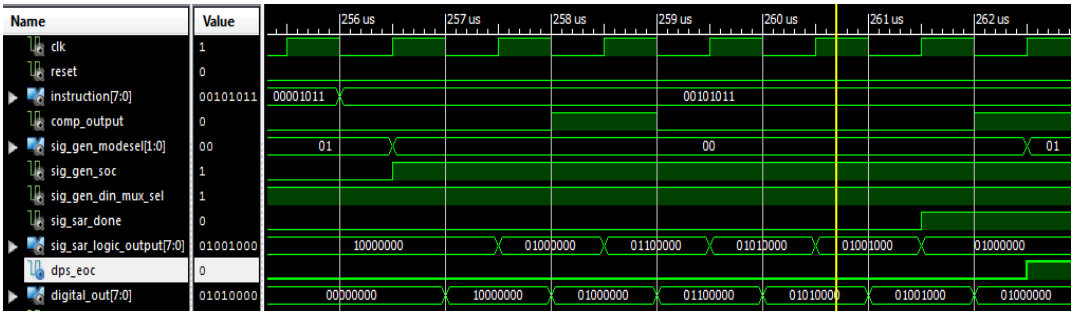


Figure 7. SAR 8-bit resolution

Similarly in figure 7, it is evident that after fourth clock cycle SAR operation halted to indicate four bit resolution operation.

[B] Pipeline Architecture

The digital section of pipeline ADC is configured by considering single bit Pipeline Architecture with feedback. The work is demonstrated with the assumption that it is interfaced with external analog section which includes a comparator, a sample and hold circuit (S/H) and a gain stage. Figure 8. and 9. depict waveforms of Pipeline architecture, configured for eight bit and four-bit

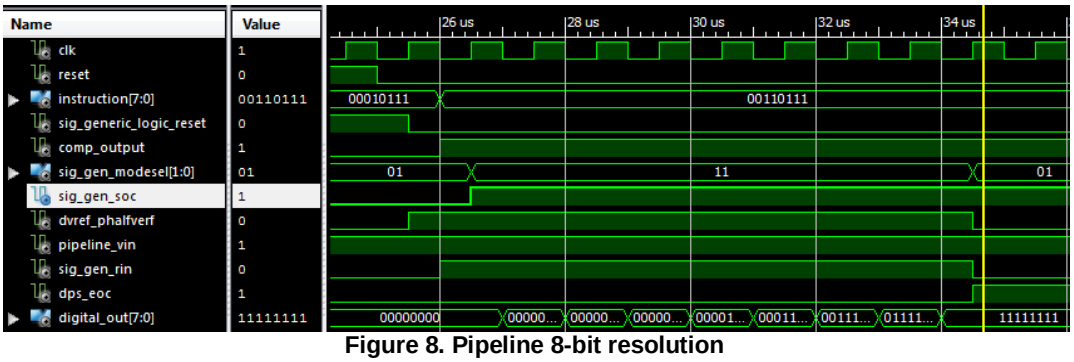


Figure 8. Pipeline 8-bit resolution

resolution respectively. Initially all bits of digital _out are zero at reset condition.
GDPU starts conversion with sig_gen_soc when 5th bit of instruction asserts. serial input, 'rin' shifted from LSB position to MSB position at every subsequent negative edge of clock. 'rin' is serial input connected to output of comparator. The end of conversion signal dps_eoc is asserted after 8 clock cycles for 8 bit resolution. In pipeline configuration, GDPU works as right serial in left shift register.

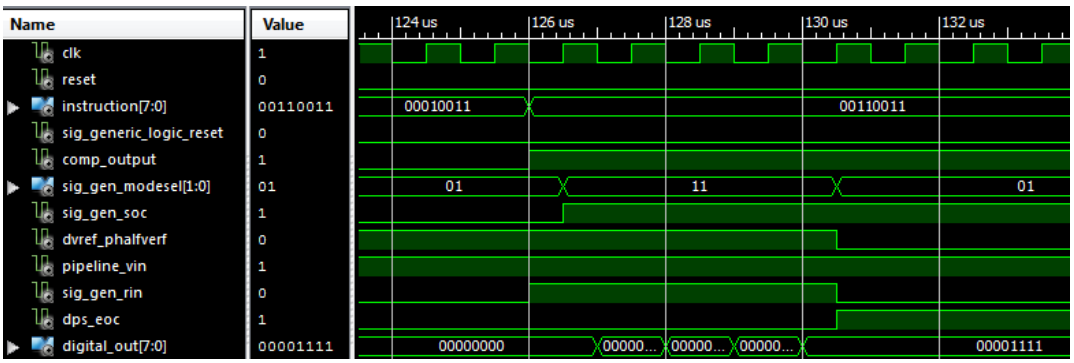


Figure 9. Pipeline 4-bit resolution

When the external comparator output is one, it indicates analog Vin > Vref/2, the MSB becomes '1' during first clock cycle. From second clock cycle onwards the successive bits are set to '1' or reset to '0', based on output status of the external analog comparator. The 'pipeline_eoc' is raised high to indicate end of conversion. It is generated by control unit (CU) when internal resolution counter reaches to the terminal count.
The 'digital_out' depicts digital output through 8 bit representations according to status external analog comparator output at consecutive clock cycles. Operational mode of GDPU is 10 after 'soc' bit till 'pipeline_'eoc'', indicating right input left shift mode of GDPU. Output is retained after end of conversion with Operational mode of GDPU is 01.

[C] Dual Slope Architecture

The system architecture is configured for dual slope ADC architecture after start of conversion signal, 'dual_slope_sw_to_vunknown' is asserted. Initially external integrator's output is connected to analog input (Vin) for stipulated time and external comparator output is one. The signal 'dual_slope_sw_to_vunknown' is disabled to zero after this timr period and another signal 'dual_slope_sw_to_vref' is set to 1, indicating external integrator is connected to vref with opposite polarity. Integrator starts loosing charge and counter in the system starts fresh counting. When entire charge is lost by integrator, external comparator becomes zero and signal 'dualslope_'eoc'' becomes one to indicate end of conversion and external integrator is reset. The count of system counter is read as digital output of the system.
Figure 10 and Figure 11 depicts timing diagram including digital output and control signals for eight bit and four-bit resolution mode respectively. The signal 'eoc' is generated after the limit of resolution space has been reached.

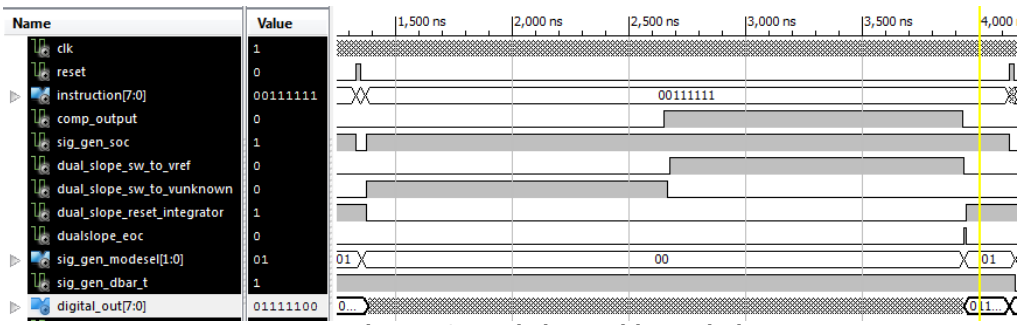


Figure 10. Dual slope 4-bit resolution

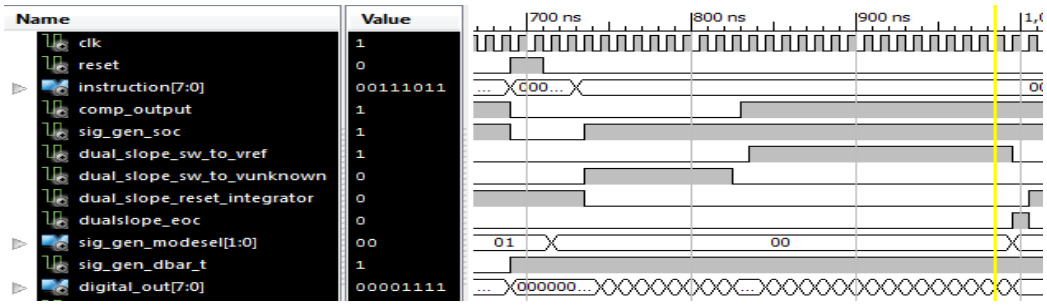


Figure 11. Dual slope 8-bit resolution

In dual slope mode operation, GDPU works in PIPO mode. At the end of conversion GDPU retains output.

[D] System Architecture Results and Comparison with Individual and Multiplexed Architecture:

Table 2 shows comparison between variable resolution reconfigurable (RC) architecture (this work) and time multiplexed digital architecture. Also, three ADCs' individual digital architectures with fixed and variable resolution are columns in the table. All architectures are implemented on common platform (FPGA 3s250ecp132-4). Time multiplexed digital architecture to be compared prominently with reconfigurable (RC) architecture (this work) as it provides three different architectures. Time multiplexed architecture provides all three mentioned types of ADCs' functionality but has explicitly all three architectures on device. Whereas RC architecture does not have any explicit architecture of any of these three types of ADCs. It is altogether new FSM based reconfigurable architecture for all these three types of ADCs.

Table2. Comparison between individual, time multiplexed and reconfigurable (RC) digital architecture Synthesized and implemented on Xilinx Spartan 3 device (3s250ecp132-4)

Sr. No.	*Parameters*	*Dual slope Fixed Reso*	*Dual slope Variable Reso*	*Pipeline Fixed Reso*	*Pipeline Variable Reso*	*SAR Fixed Reso*	*SAR Variable Reso*	*Multiplexed Variable Reso*	*This work Variable Reso. RC ADC*
1	Functionality / No. of Architectures	1/1	1/1	1/1	1/1	1/1	1/1	3/3	**3/1**
2	No. of external comparators	1	1	8	8	1	1	1	1
3	Slice Flip Flops	11	11	12	12	41	41	64	69
4	4 input LUTs	21	53	16	11	89	97	195	203
5	Synth. Clk. period(ns)	3.872	7.35	3.44	4.58	7.39	7.57	7.11	9.705
6	I/Os	19	22	18	21	13	16	29	**24**
7	PAR Clk Net skew(ns)	0.003	0.003	0.004	0.005	0.025	0.024	0.045	**0.034**
8	Total Power (W)	0.071	0.056	0.057	0.057	0.056	0.055	0.056	**0.054**
9	Dynamic power (W)	0.018	0.003	0.004	0.004	0.004	0.003	0.003	**0.001**

Figure 12 shows graphically, area utilization on target device in terms of flip-flops and number of look up tables (LUTs). It is comparable to multiplexed architecture. Figure 13 indicates synthesis clock period in ns. Figure 14 represents clock skew from place and route report. RC architecture provides lesser clock skew than that of time multiplexed architecture. Figure 15 describes number of I/O pins utilized in RC architecture and count is lesser than time multiplexed architecture. Figure 16 shows that lesser power consumed in RC architecture than multiplexed architecture. Figure 17 shows number of functionalities per architecture. Figures 14 to 17 clearly showing advantages of variable resolution reconfigurable (RC) architecture (this work) over time multiplexed architecture.

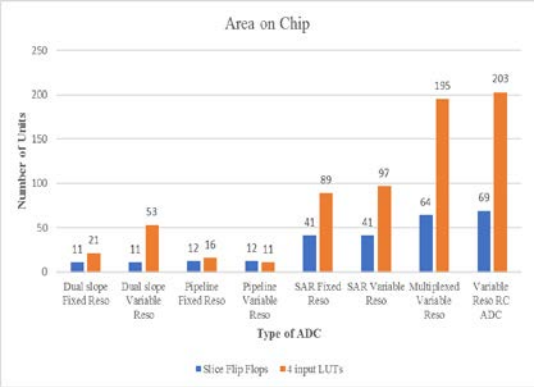


Figure 12. Area Utilization

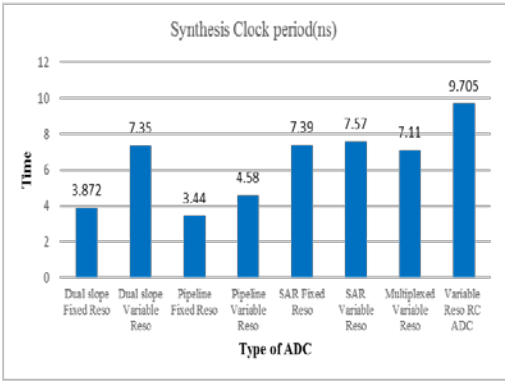


Figure 13 Synthesis Clock Period

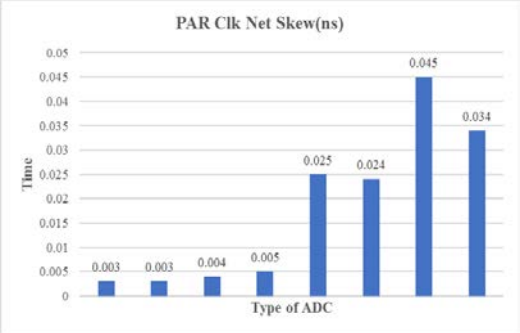


Figure 14. Clock Skew

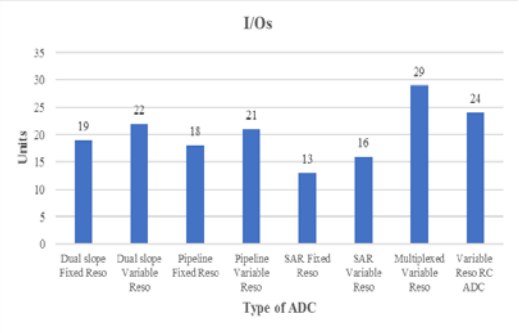


Figure 15. Number of I/O pins

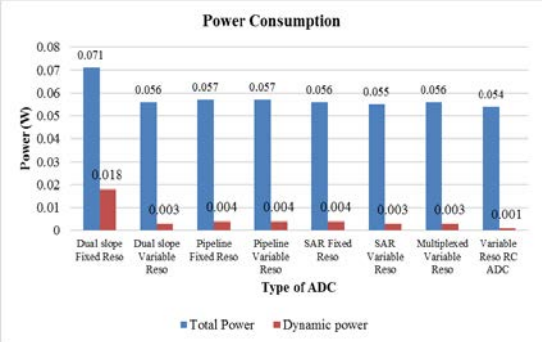


Figure 16. Power Consumption

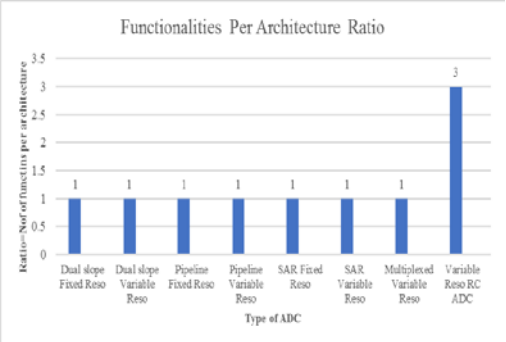


Figure 17. Number of Functionalities Per Architecture

5. CONCLUSION

The work carried out here successfully demonstrates the single reconfigurable digital output stage architecture to configure three ADC architectures viz. SAR, Pipeline with feedback and Dual slope ADCs. Specific architecture configuration is done through instruction designed specifically for it along with programmable resolution from one to eight bit. This design is based on the assumptions of the interfacing of external analog section. The architecture consumes total 0.054 W power which is lesser than that of time multiplexed architecture and can operate on maximum 30 MHz frequency without violation of timing issues and critical paths. Logic Gates utilized are 2.5 % of total gate count and 27% input output blocks of FPGA. It is evident that the architecture consumes less power and has a smaller number of input output pins requirement. Reconfigurable (RC) digital architecture exhibits lesser clock skew 0.34 nS than that of time multiplexed digital architecture. RC architecture facilitates single Comparator interface for these three types of ADCs instead of using separate comparator/s for each architecture. Hence can reduce the burden on design of analog section. Variable resolution reconfigurable (RC) architecture (this work) provides three different functionalities.

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