Estimation of Write Noise Margin for 6t SRAM Cell in CMOS 45nm technology.

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ABSTRACT:
For high speed application the static random access memory is mostly demandable. Such kind of device should possess additive parameters that can withstand during transistor scaling process. Their exist static noise margin (SNM) which degrades the device performance of memory architectures, majorly observed at write and read operation create write noise margin (WNM) and read noise margin (RNM). In this paper we discuss about the basic design of 6 transistor SRAM (6T SRAM) using 180nm and 45nm CMOS technology in Cadence Virtuoso with write noise margin analysis. The propagation delay, power dissipation, WNM are measured for both the technologies and observed that WNM is relatively low in 45nm.

KEYWORDS: SRAM, CMOS, WNM, Channel Length

1. Introduction

Microprocessors and microcontrollers with existing functioning processors are mainly used to enhance the system performance in terms of integrity and productivity. The main application of such kind of devices starts from small scale integration to ultrahigh integration with device modeling in terms of miniaturization. Especially in data application, digital evaluation and communication the most commonly used device for storage purpose is memory. In digital world the memory is classified as RAM (Random Access Memory) and ROM (Read Only Memory) that store single bit with additive functionality. Further RAM is classified as static as SRAM (Static Random-Access Memory) and dynamic as DRAM (Dynamic Random-Access Memory). When comparing with DRAM, SRAM hold's data without any requirement of external periodic refresh to store each bit, thus its performance is faster, exhibits low leakage currents [1] and typically used for high speed application. SRAM cell operates in two different states: read (*the data has been requested*) and write (*for content storage*) its design can be implemented by using CMOS-FET (Complementary Metal Oxide Semiconductor Field Effect Transistor) technology and its planar view [2] is shown in Fig.1. It contains two specified networks called pull-up and pull-down performs switching functionality using particular pMOS (p-channel MOSFET) & nMOS (n-channel MOSFET) transistors. If the silicon substrate is p-type having diffused n-type drain then it indicates as p-channel CMOS transistor purely operates when Gate voltage is low, the distance between source and drain is represented as Channel Length(L) contains high dielectric concentration. If the silicon substrate is n-type having diffused with p-type drain then it indicates as n-channel CMOS transistor purely operates when gate voltage is high. According to Moore's law for every two years the transistor count is doubled provided if the channel length (L) is scaled down (µm to nm) and consequently there is a provision of inculcating more number of transistors on a single chip.

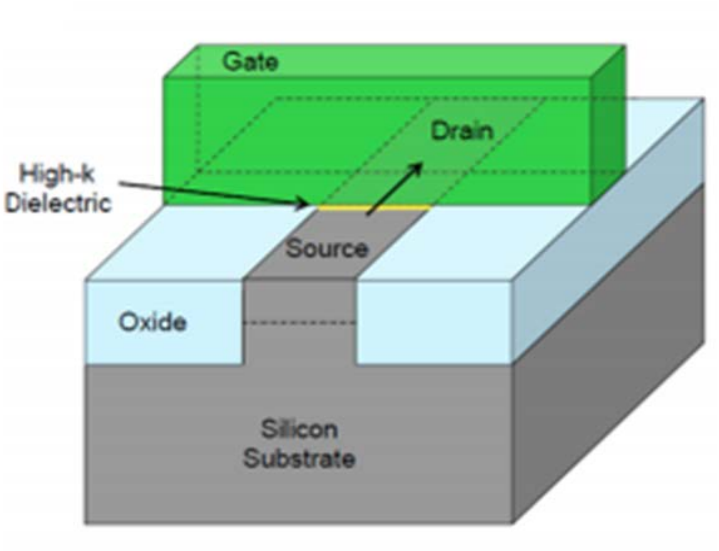

Fig.1. Planar view of CMOS transistor

2.6T SRAM

As in Fig.2 the 6T SRAM cell contains six transistors having cross-coupled inverter structure [3] formed by four transistors (*M1, M2, M3, and M4*) with two additional access transistors (M5, M6) serves as access controllers during read and write operations for storage purpose. The reduction of SRAM reliability may occur because of the wider spread of local mismatch. During active operation for the demand of minimizing power consumption, supply voltage scaling is often used. However, by operating SRAM at low voltages, the noise margin may condense further it offer good stability [4] and reliability. In this paper, we discuss about the design of standard 6T SRAM in 180 & 45nm CMOS technology with parametric analysis like Write Noise Margin {WNM}, Write delay, power consumption

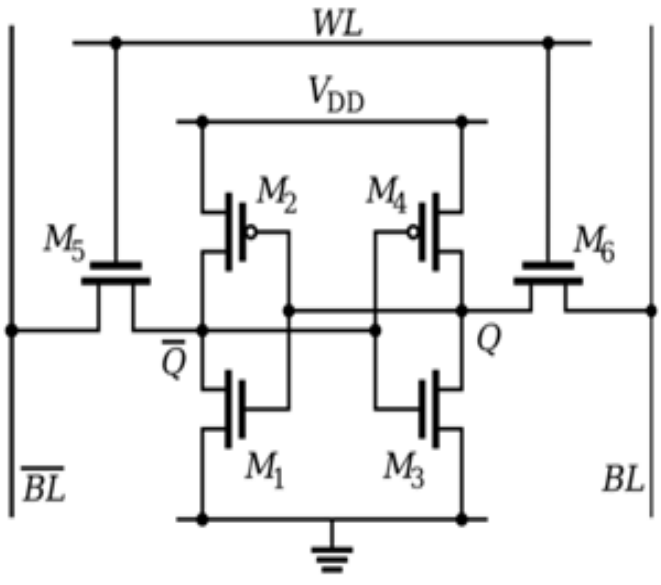

Fig.2. Standard 6T SRAM

2.1. Write-state:

In the write operation both BL, BL' act as input signals and make WL as high but when the data has accessed, then BL, BL' turn into complementary. Finally, when WL=logic high, BL & BL' are complementary, then accessed data is stored at Q and Q'

2.2. Read-state:

Read operation is carried out after the write operation and bit lines (BL, BL') are to be pre-charging to vdd, considerable a sense amplifier is used to enhance the low voltage levels to suitable logic levels(either 0 or 1) by activating read control signal to high.

3. Simulation of SRAM in CMOS 180 & 45nm technology

Schematic of 6T SRAM is shown in Fig.3 (a) is implemented in 180nm CMOS technology with global supply given as 1.8v. Only the write operation is performed: when WL is high and BL and BL' are in complementary form, then the write operation is enable by giving Q=0 & Q'=1 as in Fig.3(b) with power plot.

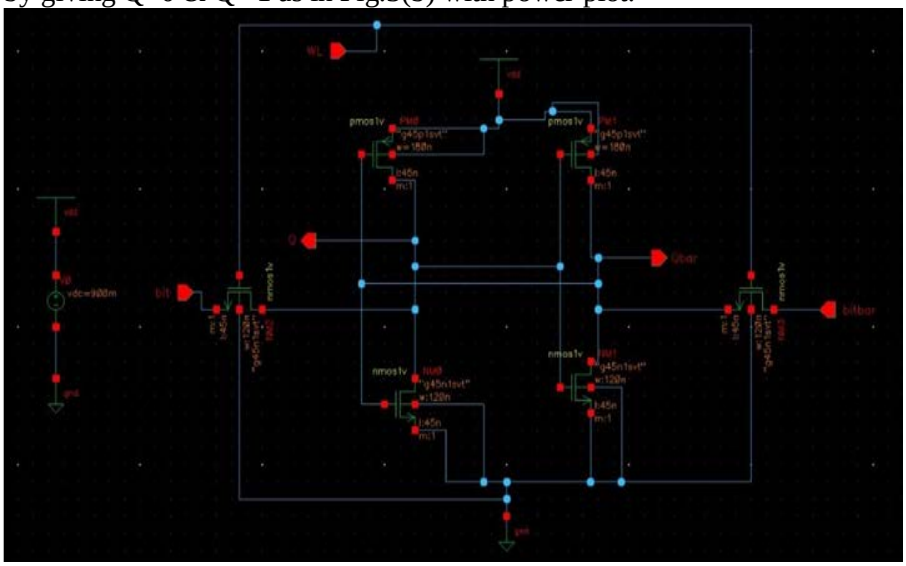

Fig.3 (a).Schematic of 6T SRAM

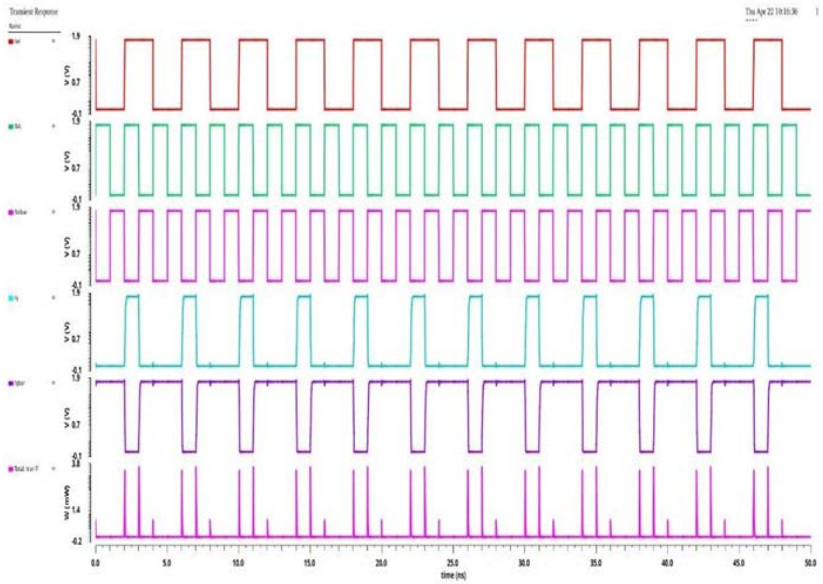

Fig.3 (b).Transient response with power plot

The write propagation delay is calculated by measuring the individual output delay at low-high and high-low states at half of the supply. The static noise margin (SNM) probably determines the noise in the SRAM cell, where as the WNM is calculated by considering the difference between W/L ratios of M4 (access transistor) & M6 (load transistor) transistor [5-6] using DC analysis, the measured value is 2.06v (at successive points of NM-low and NM-high differences) as in Fig.4.(a) based upon parasitic capacitance presented. Further the WNM can be reduced by scaling down the size of

transistor, thus the 6T SRAM is designed using 45nm to reduce parasitic capacitance value through transient simulation and all the parametric values like power dissipation, propagation delay are observed and tabulated in table.1. Finally the measured WNM is 1.118v for 0.45v in Fig.4 (b) proven better result than 180nm by considering the same W/L ratio of M4, M6 transistor.

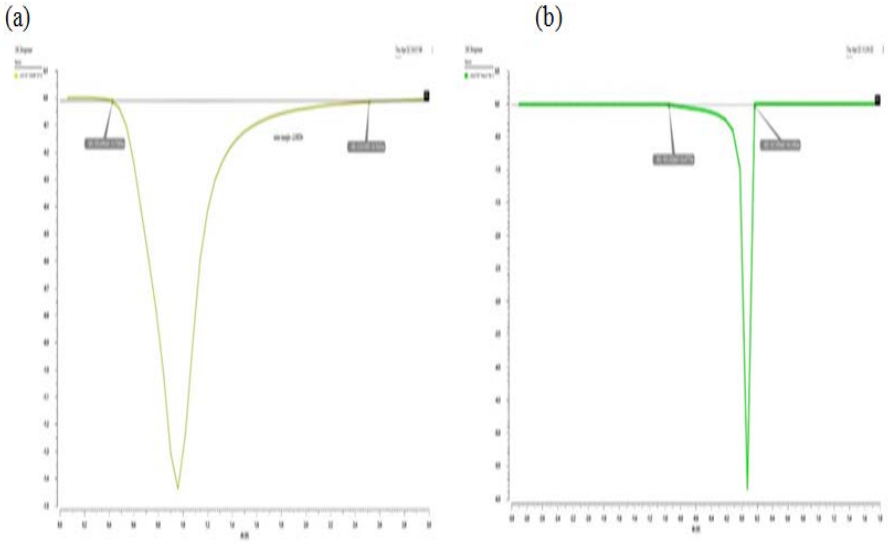

Fig.4 (a).WNM plot of 6T SRAM in CMOS 180nm. (b).CMOS 45nm.

Table.1.Performance evaluation of 6T SRAM

Technology	CMOS 180nm	CMOS 45nm
Design	6T SRAM	6T SRAM
Supply voltage	1.8v	0.45v
Write Propagation delay(ns)	2.0605	1.0359
Power dissipation(w)	45.95µ	505.7n
Write Noise Margin-WNM (v)	2.06	1.18

Conclusion

In this present research all the simulation results are taken from Cadence Virtuoso Environment. We also analyzed the write noise margin by considering the aspect ratio of access and load transistor (W/L ratio of M6 >3-4times of M4 W/L value) and observed that designed 6T SRAM in 45nm produces reduced write noise margin. Further the read noise level can be analyzed by establishing additive pre-charge and sense amplifier circuit to 6T SRAM.

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