

Comparison of Dynamic Voltage Scaling(DVS) of Core Voltage Using the On-board Voltage Regulator and External Voltage Regulator via I2C Protocol in Automotive Microcontroller

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Abstract: Dynamic Voltage Scaling is performed on automotive micro-controller AURIX from Infineon Technologies. In this micro-controller the core and different IPs operates on the 1.25 V supply rail, so dynamically voltage is changed according to the workload in the micro-controller. DVS is done either using internal onboard voltage regulator or External voltage regulator. An External board (KITPF3000FRDMEV), which has a controller and a Power Management Integrated Circuit (PMIC) is used for changing the supply voltage to the micro-controller during DVS using external voltage regulator. Micro-controller is predicting the workload and according to workload, the control command is sent to the controller (FRDM-KL25) in the kit through I2C communication and then the controller sends the command to adjust the voltage of PMIC (PF3000) through I2C communication. Both current measurements for internal voltage regulator and external voltage regulator are measured for various loads and latency is measured for various baud rates while using external voltage regulator through I2C protocol.

Keywords— Dynamic Voltage Scaling (DVS), Power Management Integrated Circuit (PMIC), Adaptive Voltage Scaling(AVS), Flexible Voltage Scaling(FVS), Low Drop Out regulator(LDO).

I. INTRODUCTION

Power consumption is becoming the limiting factor in automotive because the development in battery technology is quite slow in comparison to the increasing demand of computation and communication in automobiles. So, it is essential to utilize the available energy as efficient as possible. Micro-controllers in car for the most part have a computational stack which has time shifting characteristics. Micro-controllers in versatile gadgets have the clashing necessities to supply both ever expanding execution and ever diminishing vitality utilization. A method called Dynamic Voltage Scaling (DVS) and frequency scaling addresses these prerequisites by misusing the computational burstiness in these gadgets. By changing the core voltage and clock frequency depending upon load, vitality utilization can be minimized. DVS gives the most elevated conceivable execution when required whereas minimizing the energy utilization amid the remaining

low execution periods. The prediction of the workload of $(n+1)$ th iteration in the micro-controller depends only on the n th iteration workload not on the past iteration workload, this is known as Markov Algorithm [3]. Workload Prediction is performed on the basis of clock. If the clock for a particular module is active means that module is active and then, calculating the no of active modules which is needed to calculate the supply voltage required for safe operation. Dynamic Voltage Scaling through external board gives wider range for controlling the operating voltage and it will save the power consumption in micro controller [2]. This technique has applications like protecting the micro-controller from overshoots and undershoots, dynamically changing the voltage and frequency in automobiles, mobiles and many other low-power microprocessors. The peak performance of the micro-controller is achieved when there is a maximum utilization of power. Various techniques like Flexible Voltage Scaling(FVS) and Adaptive Voltage Scaling (AVS) addresses the peak efficiency and low power consumption in portable devices[1].Dynamic voltage scaling is the base for above techniques and it also gives the throughput boost at nominal voltage and energy reduction in comparison with other scaling techniques[2].The power management integrated circuit has got more importance in the past few years because the low power system on chip often uses multiple voltage domains with voltage scaling techniques to minimize power dissipation [3][4][5][6].Usually PMIC consist of Pre-regulators(switching regulators) and LDO(post regulators) which are used to step up and step down the voltage required for various application[9][10]. The effect of LDO on system power using the DVS is given in [7][8].

II. DVS OVERVIEW

There are two types of voltage scaling a) Static Voltage Scaling (SVS) is changing of device core voltage based on the characteristic like speed, process. It is one-time change done during the boot up time. b) Dynamic Voltage Scaling (DVS) is the changing of device core voltage based on the operating workloads (No of active modules). Here Voltage is dynamically varied throughout the device operation. In Infineon Aurix micro-controller, DVS consist of two critical process called load jump and voltage Droop. Load jump is a process which occurs in micro-controller when many modules in micro-controller are enabled or disabled (based on active clock signal) i.e. CPU are either in idle state or in run state or multiple CPU's are disabled. When Load jump happens the core voltage VDD can cross the overshoot and undershoot voltage value. Load jump has two possible results i.e., positive load jump and negative load jump. When significant no of modules are enabled i.e. CPU $x(x=1,2,3)$ are in run state, it is called as Positive load Jump. similarly, when large no of modules is disabled, it is called Negative load jump. The consequence of Positive load jump is that the VDD core voltage may drop below so that it can reach below the undershoot voltage value due to large no of active modules. similarly, for Negative load jump VDD core voltage may increase too much above the overshoot voltage value due to large no of inactive modules. To overcome Load jump, Voltage Droop is performed, i.e., just before the negative load jump, the core voltage VDD is decreased by some value (Like in this experiment 80mV) (as overshoot and undershoot value is chosen based on Power specification) and similarly just before positive load jump, the core voltage VDD is increased by 80 mV.

III. Hardware Architecture

AURIX micro-controller is an Automotive micro-controller which has an inbuilt (onboard) voltage regulator for the core voltage supply rail, which automatically detects the Load Jump using the monitor circuits and performs the Voltage Droop. To perform the DVS using external Voltage regulator, the onboard internal voltage regulator has to be disabled and the supply core voltage VDD has to be supplied from the external PMIC voltage out. Hardware architecture for DVS is shown in Fig 1. Here Automotive micro-controller used is Tricore Aurix from Infineon family which has core voltage VDD supply rail of 1.25V. Aurix micro-controller is connected to external Voltage regulator

Kit PF3000 which supports I2C protocol for communication. Aurix micro-controller predicts the workload (no of active cores/IP modules) and sends the command to controller present in PF3000 which modifies the required core voltage VDD. AURIX micro-controller takes three various voltage levels for operation. 5V and 3V to power up onboard supporting modules and Flash respectively. 1.25V is used to power the core voltage.

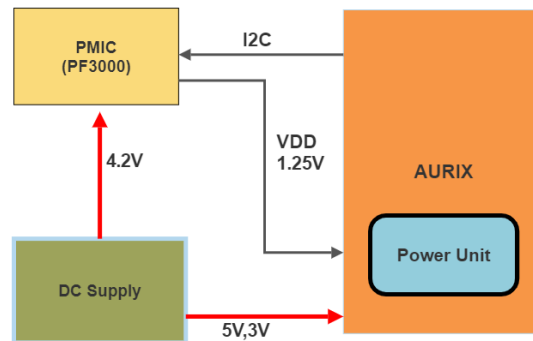


Fig. 1. Hardware architecture for DVS using external voltage regulator.

IV. IPC State Machine

Finite State Machine (FSM) is implemented for controlling the voltage of CPU core by voltage scaling using external Voltage regulator (PF3000). FSM will check core voltage and temperature for safe operation. There are four important different states in FSM as shown in Fig 2.

- a) **START**- It is used to initialize FSM.
- b) **RAMP**-It is used to perform voltage scaling by increasing the voltage of core in steps(10mV) until the desired voltage level is achieved.
- c) **PARK**-In this state core voltage and core temperature is checked if the voltage and temperature are within specified level. If there is any error in this state, then the FSM is terminated. Operating voltage level (1.15V to 1.30V) and the operating temperature level (-40°C to 130°C).
- d) **SAFE**-This state ensures that one complete cycle of Voltage scaling is performed successfully.

V. Measurements & Results

DVS is performed on Automotive micro-controller using onboard voltage regulator and by using external PMIC kit PF3000 for external Voltage regulator. Fig 3 shows the positive Voltage Droop with an interrupt pin shown in blue color which is high during positive Droop process. Similarly, Fig 4 shows the Negative Voltage Droop.

Fig 3 and 4 shows the Voltage Droop concept without varying load.

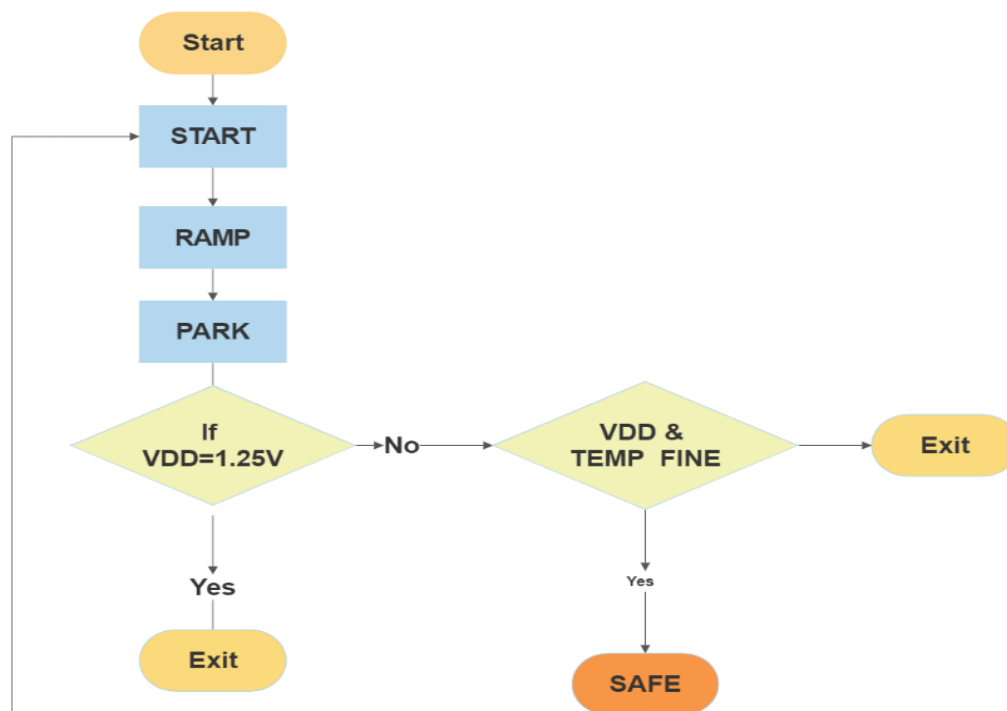


Fig. 2. Flow chart for the Finite State Machine

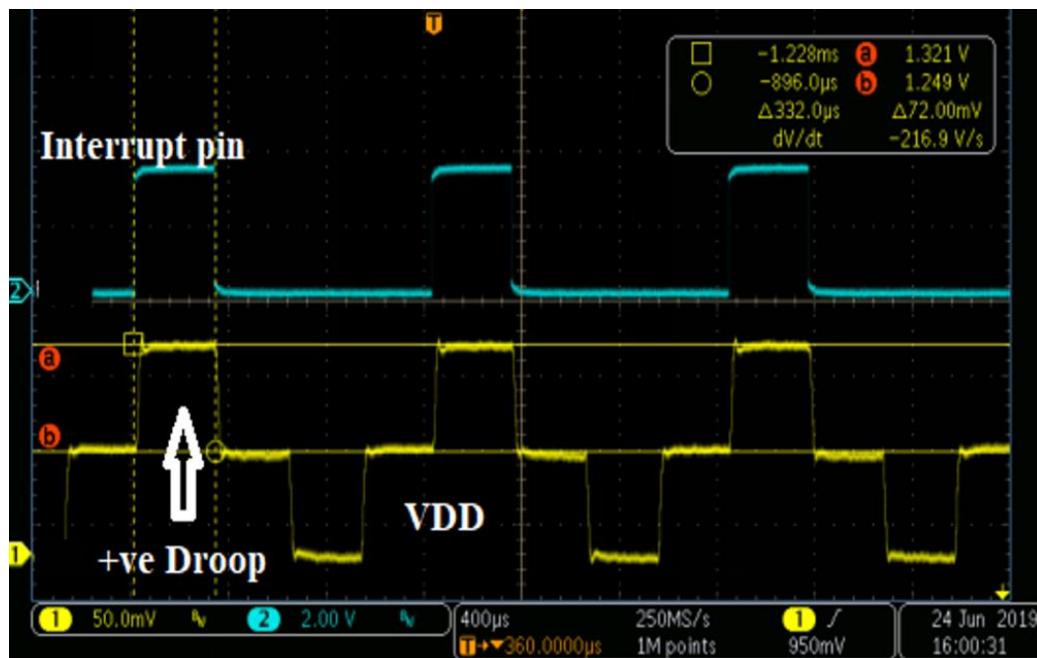


Fig. 3. Positive Voltage Droop

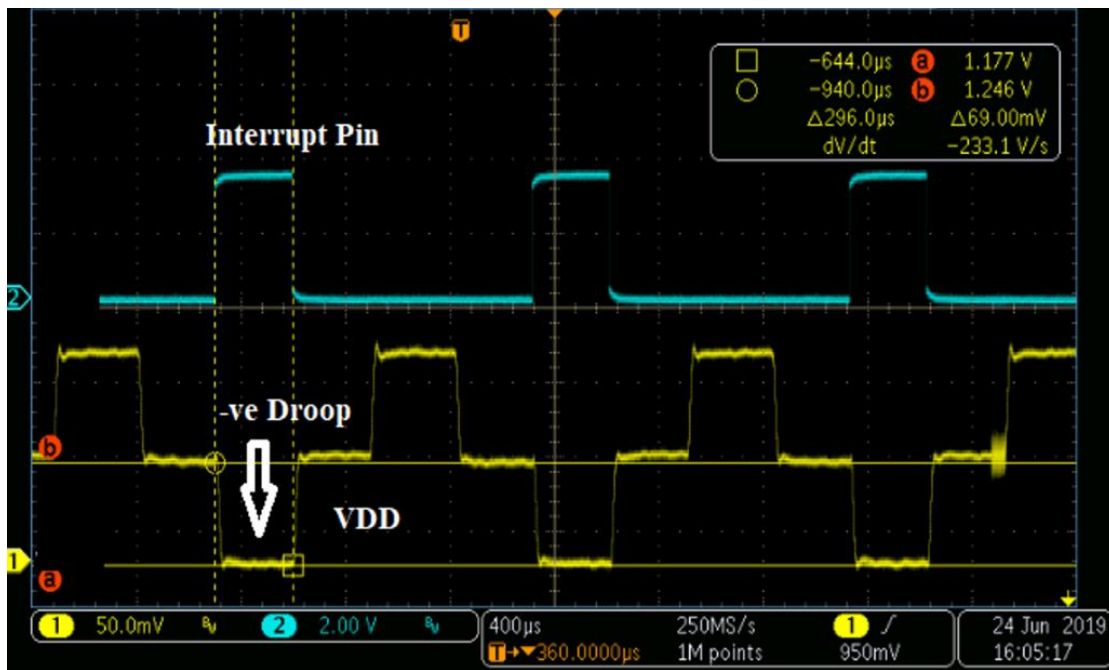


Fig. 4. Negative Voltage Droop

Fig 5 and 6 shows the actual voltage Droop using the onboard voltage regulator. Here, it is observed that the VDD voltage fluctuation highlighted in the blue box showing the Positive Voltage Droop.

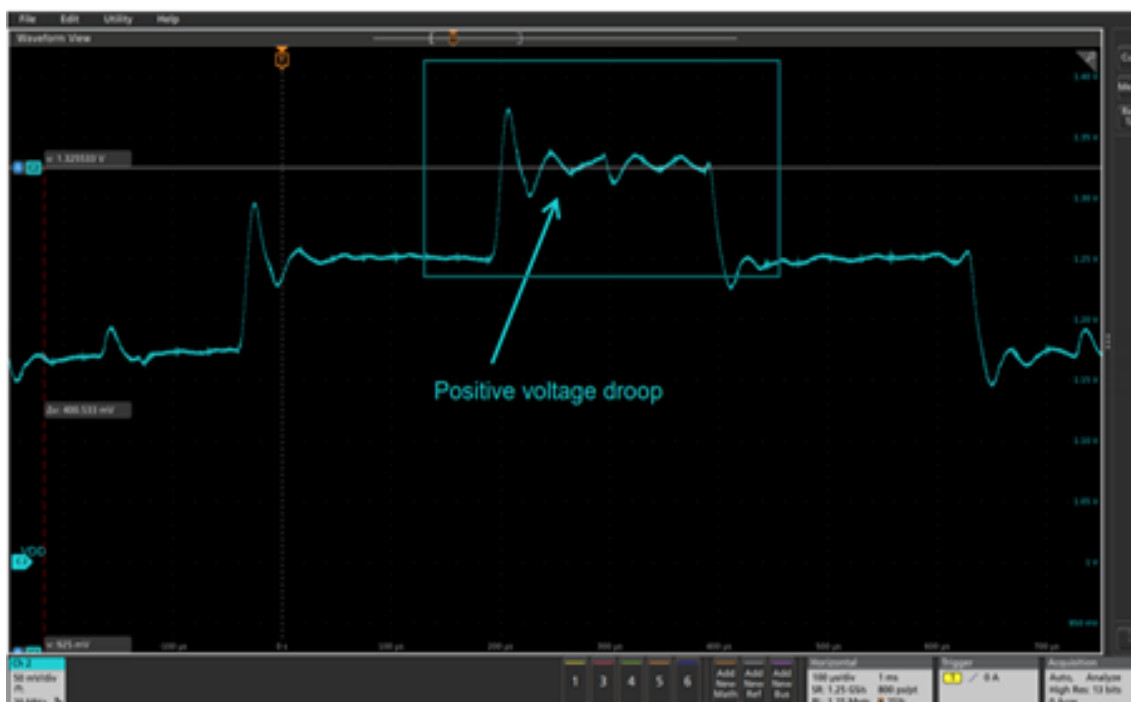


Fig. 5. Positive Voltage Droop with Load

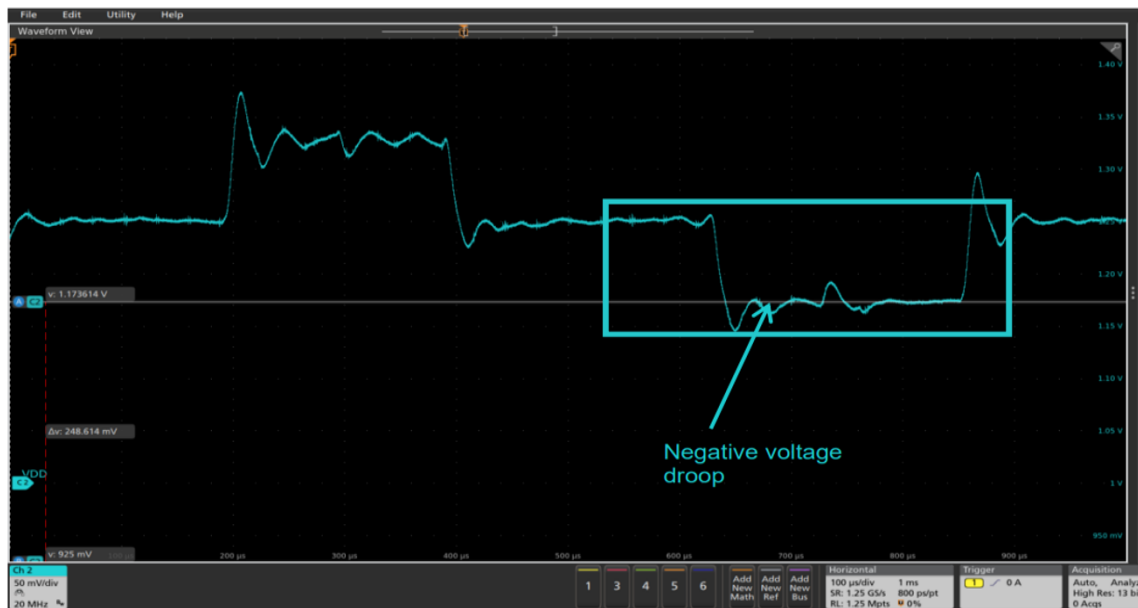


Fig. 6. Negative Voltage Droop with Load

Fig 7 and 8 show the actual Voltage Droop with load jump using external Voltage regulator through I2C. It also includes the corresponding Load Jump shown in yellow colour. The core voltage VDD is shown in blue colour.



Fig. 7. Positive Droop with Negative Load Jump using External Voltage Regulator

Fig 9, 10 and 11 show the FSM output for various states based on the FSM which verifies DVS. Fig 9 shows the Positive Voltage Droop success message in the end. The starting Voltage considered is 3V and the final voltage is 6V. Droop of 3V is performed.



Fig. 8. Negative Droop with Positive Load Jump using External Voltage regulator

Similarly, Fig 10 shows the Negative Voltage Droop success message in the end. The starting Voltage considered is 3V and the final voltage is 1. Droop of 2V is performed. Fig 11 shows the unsuccessful Droop output due to exceed in temperature. Since temperature value is 145C, Droop failed.

```
Initial voltage=3volts
choose droop 1.positive droop 2.negative droop1
DVC_start is initialized
DVC_ramp is initialized
DVC_park is initialized
DVC_safe is initialized
Vdd = 4, Temperature = 132
DVC_start is initialized
DVC_ramp is initialized
DVC_park is initialized
DVC_safe is initialized
Vdd = 5, Temperature = 132
DVC_start is initialized
DVC_ramp is initialized
DVC_park is initialized

droop successfull
vdd=6
temperature=132
-----
```

Fig. 9. FSM output for Positive Droop success

When external voltage regulator is used for voltage scaling there will be some latency due to I2C communication. In Fig 12 it is observed that the P26-2 pin goes high instantly due to droop request but the actual VDD voltage from External PMIC out has some delay due to I2C latency.

```
Initial voltage=3volts
choose droop 1.positive droop 2.negative droop2
DVC_start is initialized
DVC_ramp is initialized
DVC_park is initialized
DVC_safe is initialized
Vdd = 2, Temperature = 84
DVC_start is initialized
DVC_ramp is initialized
DVC_park is initialized

droop successfull
vdd=1
temperature=84
-----
```

Fig. 10. FSM output for Negative Droop success

```
Initial voltage=3volts
choose droop 1.positive droop 2.negative droop1
DVC_start is initialized
DVC_ramp is initialized
DVC_park is initialized
temperature is exceeded....temperature=145
droop not successfull
-----
```

Fig. 11. FSM output for Droop failure

When external voltage regulator is used for voltage scaling there will be some latency due to I2C communication. In Fig 12 it is observed that the P26-0 pin goes high instantly due to droop request but the actual VDD voltage from External PMIC out has some delay due to I2C latency.

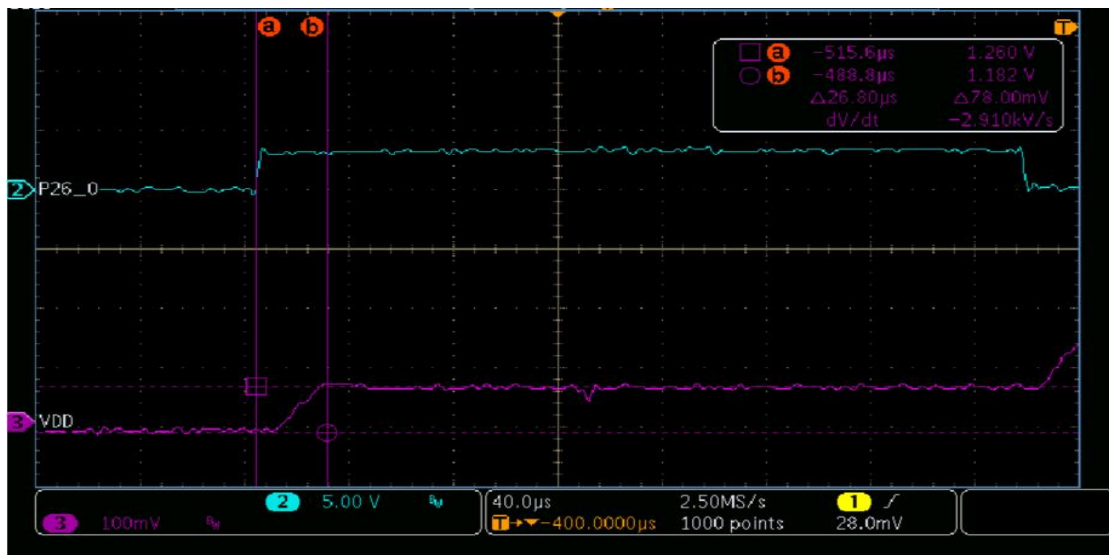


Fig. 12. Latency graph of VDD using external Voltage regulator

Table 1 shows the various Latency values for various Baud rates chosen for I2C communication. It is observed that as the Baud rate increases delay decreases.

Table 1 Latency Vs Baud Rate

Baud rate (in kHz)	Delay change in VDD (in microseconds)
97	80
129	25.20
148	24.80
228	22.80
253	22.40
293	22.10

Table 2 shows the Current measurement to compare the Voltage scaling using the internal and external Voltage regulator. Here two CPUs are taken under consideration.

Table 2 Current report for internal and external voltage regulator

State	IDD (mA) (internal)	IDD (mA) (external)
Before Negative Voltage Droop	211	235.355
Negative Voltage Droop	196.439	219.896
CPU1 in Sleep Mode	189	210.834
CPU2 in Sleep Mode	182	206.768
Modules Clock Disable	128	148.468
Before Positive voltage Droop	140	159.129
Positive Voltage Droop	150	171.389
CPU1 in Run Mode	159	181.517
CPU2 in Run Mode	168	195.909
Modules Clock Enable	230	251.879

It is observed that the Voltage scaling using external voltage regulator consumes more power due to I2C interface and it also introduces Latency.

VI. CONCLUSION

The conclusions from the hardware implementation of Dynamic Voltage Scaling are as follows:

- a) Dynamically changing the voltage through Power Management Integrated Circuit (using External regulator) provides wider range of control of VDD voltage.
- b) DVS using External voltage regulator can protect the micro-controller from overshoot and undershoot.
- c) A module in AURIX is active when its clock is enabled. So, workload monitoring has been done on the basis of checking the clock for particular module.

VII. FUTURE SCOPE

- a) To perform Dynamic Voltage Frequency Scaling on Microcontroller.
- b) To apply machine learning in predicting the workload for Aurix.

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