# Design and implementation of Dual-Port Memory

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***Abstract:***
*Multiport memory cell using a dual-port memory cell provides required access to multi-processor-based applications. Simultaneous access can be provided using two-pass transistors, pair of bit lines, and a word line. Using specific word lines and bit lines of SRAM cell access can be provided by using dual ports memory. The single address of a memory cell can be accessed at a time during each clock pulse using single-port SRAM this drawback can be overcome by using dual-port RAM which supports concurrent read or write access at different addresses. Efficiency is improved by using dual-port RAM. Each processor can be made to operate at different clock frequencies thereby dual-port RAM will not have any limitations of access between the two ports.*

***Keywords:*** Dual port memory, power consumption, write/read access, single port memory, Word line, bit line.

## 1. INTRODUCTION

SRAM memories are the primary element of System-On-Chip (SOC). SRAM systems suffer from the disadvantage that they occupy more area which affects power and the yield. Frequently, the memories are implemented using SRAMs as they are robust, have high speed, and can be readily incorporated into logic circuits. Conceptually memory is an array of storage registers with distinct addresses, which is a number identifying the location. Memory addresses usually start at zero and increases by one for each location up to one less than the number of locations. Power of 2 is the number of locations for most of the memory components. Addresses ranging from 0 to $2^{n-1}$ requiring an n bit address to represent a memory with $2^n$ locations. The total no of bits in the memory component is $2^n$ x m, if each location stores m bit of encoded information

## 2. LITERATURE SURVEY

A new P-MBIST with the aim of merging the FSM and Microcode architecture using macro-commands is proposed. The hybrid P-MBIST utilizes the same macro-commands for selecting the test algorithm and same encoding technique for the MARCH elements but instead of using state machines, it is designed by implementing clusters of microcode to control the read/write operation and test data injection. [1]

EDA industry is see-king maintenance methodologies to support its software, and to improve the overall quality of tools as they are affecting customer satisfaction. Monitoring activities of tools and detecting post development software errors cannot be overestimated. The experiments show the ability of the TMB Validator to verify various controller features and demonstrate its versatility to determine reliably when working with a variety of memory fault models. [2]

The Current March Algorithm with 22 N is inefficient in certain cases to make a full diagnosis of SRAM. The proposed scheme is more efficient in terms of circuit size and test data to be applied, and it requires less time to test SRAM chip. [3]

The area occupied by embedded recollections in System-on-Chip (SoC) is over 90%, and expected to elevate up to 94% by 2014. Thus, the performance and yield of embedded recollections will dominate that of SoCs. SRAM is more expensive and less dense than DRAM and is therefore not used for high capacity, low cost applications such as the main memory in personal computers. [4]Programmable BIST approaches, allowing selecting after fabrication a large variety of memory tests, are therefore desirable, but may lead on unacceptable area cost. BIST approaches enabling test algorithm program ability and data background program ability at low area cost have been presented in the past. However, no proposals exist for programming the address sequence used by the test. [5]

## 3. METHODOLOGY

Single-port memories will be having only one port for reading and writing data. The data connections can be separated into output and input connections, and it will have only one address input. A read or write operation is only possible with reference to single-port memory which can provide only one access at a time. [6]

To overcome the disadvantage associated with single-port memories, we have designed multi-port memories. Multi-port memories will have many address inputs with corresponding data inputs and outputs. Concurrent operation depends on the number of input address line. Dual-port memory is the most common type of multi-port memory. Area consumption of multi-port memory is more compared to single-port memory with same number of bits of storage, the reason for this is multi-port memories consists of separate address decoder and data multiplexers for each access port. [7]

Additional wiring will be required to connect the cells to the access the port, and the internal storage is shared with the memories. Additional cost can be justified for many applications like high-speed network connections and high performance graphics processing. [8]

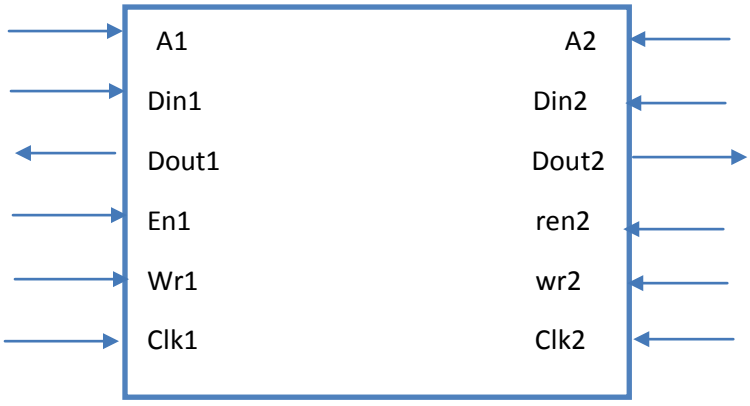



Figure 1: Dual port RAM

Let us consider a scenario in which we have a subsystem which produces the data for storing the data in memory and another subsystem to access the data to process it. If we implement the above system using single-port memory we have an additional task of multiplexing the data and address of the subsystem with the memory. The arrangements of the control section has to be made in such a way that it has to take turns to access the memory. [9]

Now let us discuss the problems associated with the mentioned technique, the memory becomes a bottle neck when the total rate of moving the data in and out of the subsystem exceed the overall rate. If have more than one subsystems and two systems have a requirement of having access to memory at the same time then there will be loss of data. The solution to the mentioned problem is to incorporate separate access ports for subsystems.

In asynchronous dual-port memory simultaneous access results in delayed response. If the operation is write and if the two subsystems try's to perform it simultaneously then it will result in unpredictable results getting stored in memories. Multi-port memories manufactured in the form of packaging components can avoid this issues by using additional circuits to indicate the time at which contention take places.

## 4. RESULTS

The Dual-port memory design is performed using cadence software. 64k dual-port memory of capacity 8bits is designed. It consists of 12 address lines and 8 data lines. The operation of the circuits can be explained considering the following cases, we have to demonstrate the usage of dual-port memories. When the wr_en is high it signifies the write operation and when wr_en is low it signifies read operation. We have configure one of the port to have both write and read access and the other port is provided only with read aceess. Port_en is used to activate the two ports.

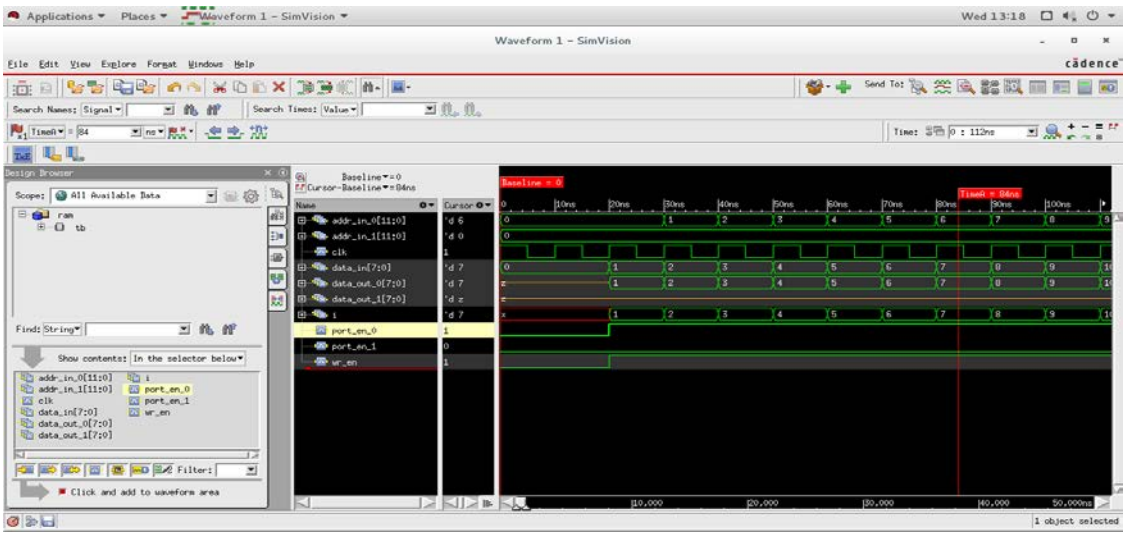
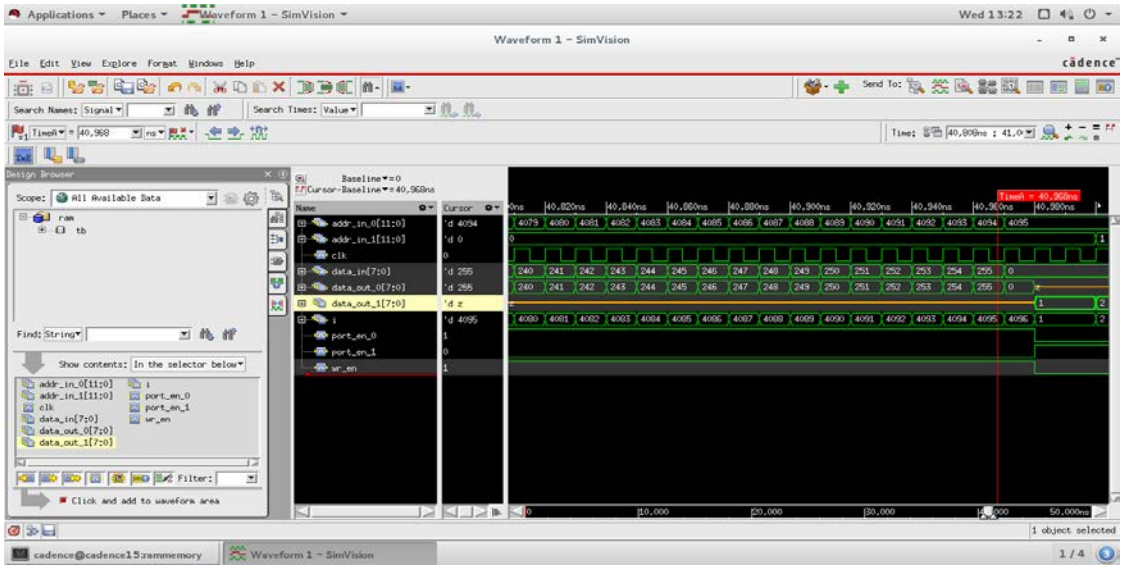



Figure 2: Simulation of Dual-port memory to show write operation at port 0 address.

We can see from figure 2, write operation is performed at the initial address by having a value of wr_en high, the value of the input available at the data_in is available at the data_out after the application of the clock pulse. This shows the proper read operation of the dual-port memory.




We can see from figure 3, write operation is performed at the last address by having a value of wr_en high, the value of the input is available at the data_in are available at the data_out after the clock.

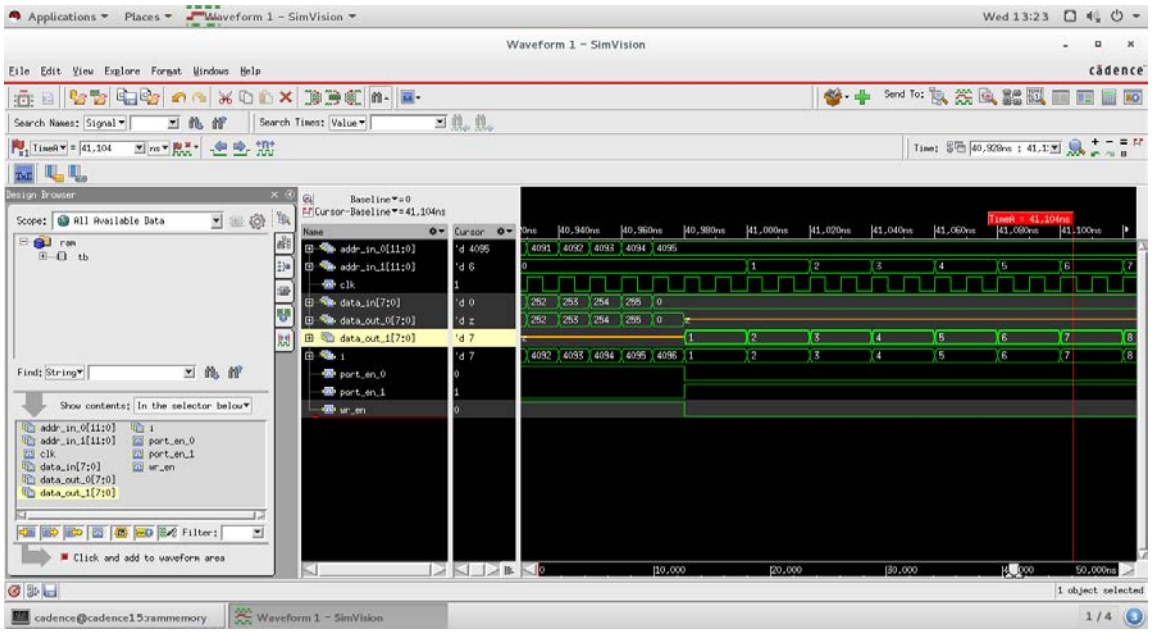



Figure 4: Simulation of Dual-port memory to show read operation at port 1 initial address.

We can see from figure 4, read operation is performed at the initial address by having a value of wr_en low, the value of the data available in the memory is outputted to data_out after the application of the clock.

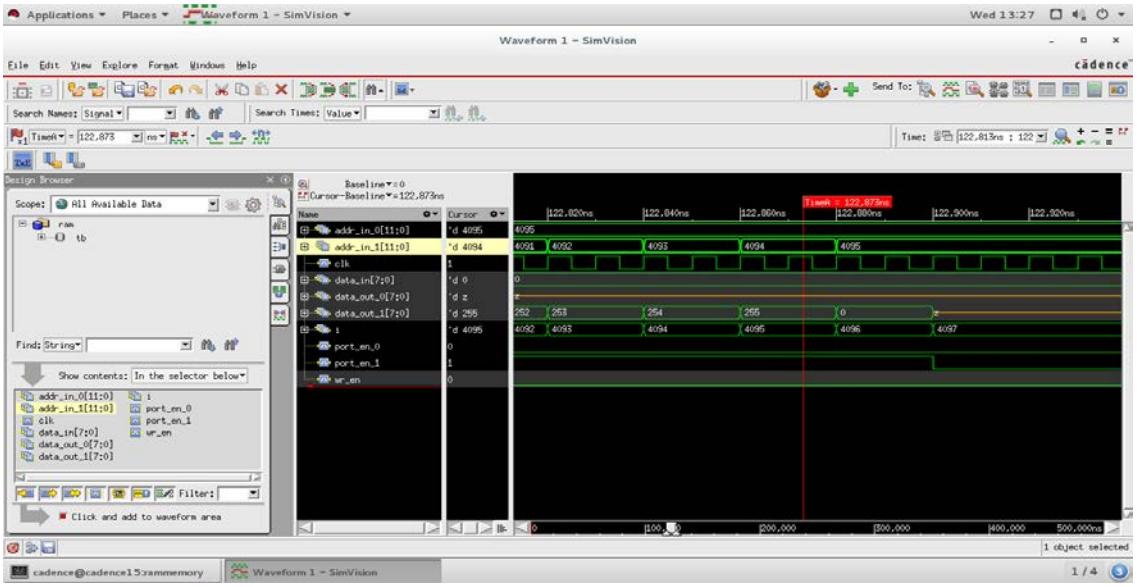



Figure 5: Simulation of Dual-port memory to show read operation at port 1 final address.

We can see from figure 4, read operation is performed at the final address by having a value of wr_en low, the value of the data available in the memory is outputted to data_out after the application of the clock.The design is synthesized and the RTL of the dual-port memory is shown in figure 6. The area, power and timing of the dual-port memory is provided.

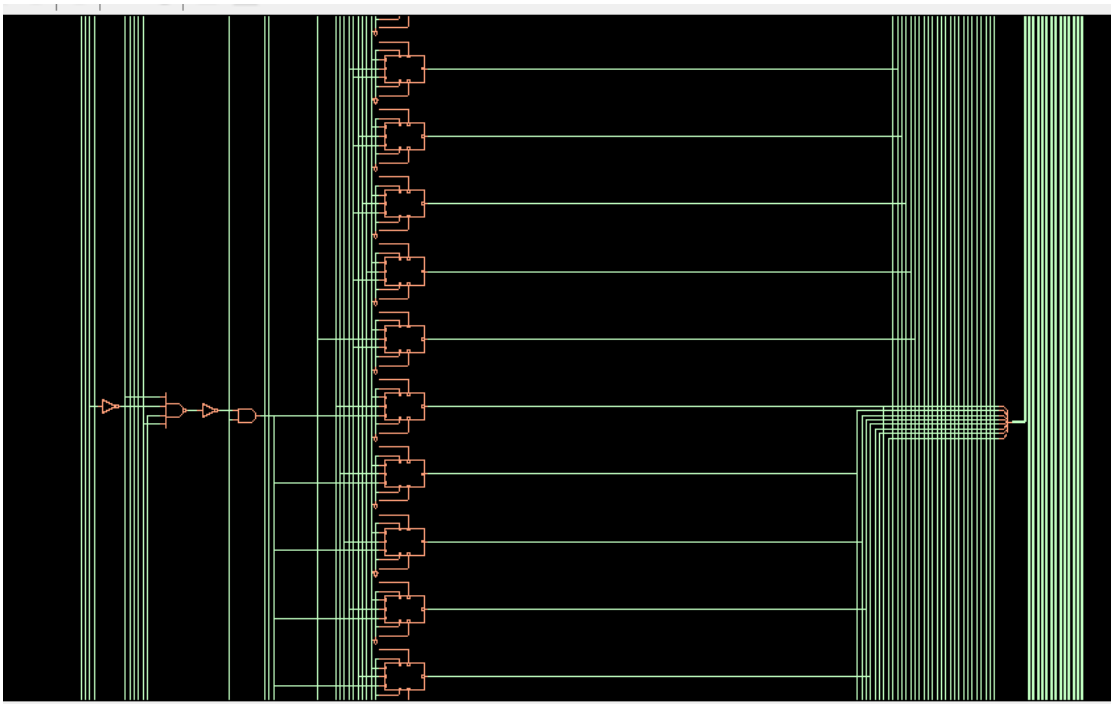


Figure 6: RTL of Dual-port memory

| Pin | | Type | Fanout | Load (fF) | Slew (ps) | Delay (ps) | Arrival (ps) | |
|---|---|---|---|---|---|---|---|---|
| ram_reg[15][0]/clk | | | | | 0 | | 0 | R |
| ram_reg[15][0]/q | (u) | unmapped_d_flop | 2 | 2.0 | 0 | +318 | 318 | R |
| mux_ram[addr_in_1]_44_45/in_15[0] | | | | | | | | |
| g8/data15 | | | | | | +0 | 318 | |
| g8/z | (u) | unmapped_bmux20 | 1 | 1.0 | 0 | +484 | 803 | R |
| mux_ram[addr_in_1]_44_45/z[0] | | | | | | | | |
| g297/in_0 | | | | | | +0 | 803 | |
| g297/z | (u) | unmapped_bufif1 | 1 | 0.0 | 0 | +17 | 820 | R |
| data_out_1[0] | | interconnect | | | 0 | +0 | 820 | R |
| | | out port | | | | +0 | 820 | R |

Figure 7: Timing report of Dual-port memory

| Instance | Cells | Leakage Power(nW) | Dynamic Power(nW) | Total Power(nW) |
|---|---|---|---|---|
| dual_port_ram | 213 | 20.888 | 5588.220 | 5609.109 |
| mux_ram[addr_in_1]_44_45 | 8 | 3.675 | 397.925 | 401.600 |
| mux_ram[addr_in_0]_42_45 | 8 | 3.675 | 382.886 | 386.561 |

Figure 8: Power report of Dual-port memory

| Instance | Module | Cells | Cell Area | Net Area | Total Area | Wireload |
|---|---|---|---|---|---|---|
| dual_port_ram | | 213 | 2079 | 0 | 2079 | <none> (D) |
| mux_ram[addr_in_0]_42_45 | bmux | 8 | 342 | 0 | 342 | <none> (D) |
| mux_ram[addr_in_1]_44_45 | bmux | 8 | 342 | 0 | 342 | <none> (D) |

Figure 9: Area report of Dual-port memory

## 5. CONCLUSION

The implementation of dual-port memories provides simultaneous access to read and write operation concurrently and the only drawback is the increased amount of area required for implementation of dual-port memory. The dual-port memories is successfully implemented and tested using cadence software.

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