Implementation of LPDDR4 Memory Interface Using AXI3 Protocol with Optimization Technique

Gopalakrishna P
Dept of ECE
BNMIT, Bengaluru, India

Dr. P. A. Vijaya
Professor and Head, Dept of ECE
BNMIT, Bengaluru

***Abstract* --- In electronics one of complex design is SOC (system on chip) design, where many of the predefined or IP (intellectual property) circuit which can be analog, digital or mixed signal will be combined each other and said that many circuit is combined to a single chip. In this paper it is been designed the low power double data rate version of 4 memory (LPDDR4). It is one of the SDRAM architecture and since it is a memory there should be required a protocol to read a data from memory and to write a data from the memory for that purpose a AXI3 protocol is been used and the memory controller is been used to check the given input from the AXI protocol is correct or not. The entire SOC design is implemented using Verilog code and checked in the Xilinx 14.7 ISE and simulation is verified then the RTL is viewed in ModelSim 10.5 tool and verified the code coverage of design and testbench.**

I. INTRODUCTION

The SOC is of creating many ICs (Integrated Circuits) by combining transistors on one single chip is called VLSI (Very Large Scale Integration). Here Hardware description programming language like Verilog, System Verilog or VHDL is used to describe the ICsfunctionality. VLSI technology been started in the year of 1970s at that time there was developing a, communication chips, compound semiconductors and earliest microprocessors. Before the introduction of VLSI technology, most ICs performed a fixed and limited set of design functions were used. VLSI technology is very helpful to designers to design a memory blocks such as flash memory,ROM etc.
In VLSI technology SoCdefines a specific design flow they are, ASIC(application specific integrated circuit) and FPGA (Field Programmable Gate Array) designs. To achieve the design of an integrated circuitEDA (Electronic Design Automation) tools is used in different stages in the design flow of a unique combination circuits.

The specific application design requires many more I/O of single processor, so can't meet the need of more and more I/O in the single processor for complex computational task. Hence we are able to use the suitable of protocol so that the action in the multi slave form single master will reduce the requirement of more I/O in the chip integration. Thanks to the manufacturing development of integrated circuit technology.Now as there are protocol and processing unit it is getting faster, hence it overcomes from slow communication architectures but a bit difficult furthermore this slow the conventional throughput of communication architecture.

The protocol with high-performance, high-frequency system designs and includes a number of features that make it suitable for a high-speed throughput is considered as a AXI protocol. It helps in theEnable of High Frequency operation, low-latency designs by a complex bridges and meet with the interface requirements in wide range of requirements for suitable to control a memory controllers with flexibility in high initial access of a data provided in the implementation of interconnect architectures by backward-compatible withthe interface.

The key features of the AXI3 protocol are:

- Separate address/control and data phases.
- Support for unaligned data transfers using byte strobes.
- Burst-based transactions with only start address issued.
- Separate read and write data channels to enable low-cost Direct Memory Access (DMA) ability to issue multiple outstanding addresses.
- Out-of-order transaction completion.
- Easy addition of register stages to provide timing closure.

Code coverage

Statement Coverage: It is the executable statements in the source code are executed at least once. It is used for calculation of the number of statements in source code which have been executed.

Branch coverage: It is a testing that aims to ensure that each one of the possible branch from each decision point is executed at least once and thereby ensuring that all reachable code is executed.

Toggle coverage: It reports describe design activity in terms of changes in signal values. Toggle coverage reports can identify a variety of issues in the design and the testbench

II. RELATED WORK

AbhinavTiwari, Jagdish an Efficient AXI Read and Write Channel for Memory Interface in System-on-Chip in his memory interface design have achieved a throughput with the help of DDRcontrollers [1]. The design challenges of DDR controller in FPGA, it has used the SoC FPGA.Typically, FPGA design involves connecting the IP functionalities, which is running at different frequencies of clock with standardAXI bus protocol.Thebetter way for the streaming data from throughput could be enhanced in a with help of AXI interface design.Payal M J1, R N Awale2 case study of lpddr4-phy has analysed that the AXI protocol will achieved the data transfer efficiency [2]. TheSoC FPGA AXI design bus standard requires synchronous IP interfaces for DDR different clock pulse [3]. Hence AXI protocol will be considered the best interface model to transmission the data at the higher frequency and also The AXI provides higher grade of IP capable in memory mapped interface [4]. We have used synchronous FIFO with gray to binary coders for Bus encoding architecture for low- power implementation of an AMBA-based SoC platform[6] Channel dependency handshaking is defined by the DDR3 AXI [7].AXI has separate read and write channel for data transmitting to master and write response for handshaking about the data transfer to the slave the response are OKAY,EXOKAY, SLERR AND DECERR which is mandatory for multi master slave system. To the our proposed work it is single master and single slave interconnected to increase the overall throughput by avoiding such handshake dependencies due to the write response.

III. PROPOSED ARCHITECTURE OF THE DESIGN

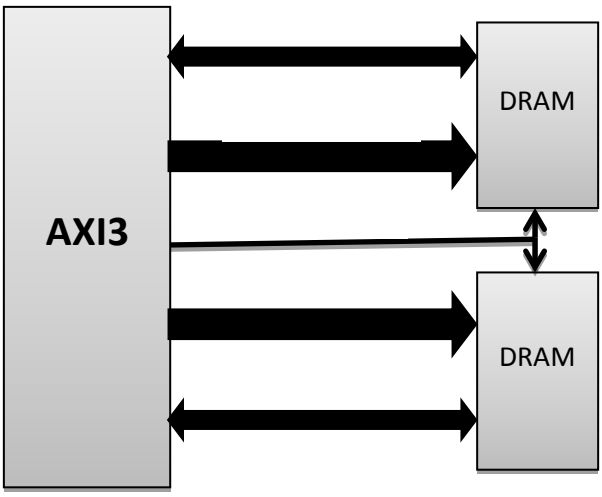

Fig1: LPDDR4 architecture

The AXI3 protocol will help in fast in the data transfer since it of a parallel connection to the data which is required to its slave part. The AXI3 protocol is considered and for slave part for memory data transfer application, the AXI3 is the parallel interconnection to its slave in this paper AXI3 slave is a LPDDR4 memory the interconnected data buses are, command/address of the memory data which is to read or write value and the chip select to select the required chip which are the LPDDR4 architecture.

LPDDR, is an Low-Power Double Data Rate, also known as Low-Power DDR SDRAM or LPDDR SDRAM, is a type of double data rate synchronous dynamic random-access memory that consumes less power and is targeted for mobile and computers. It is two different DRAM hence at a time only half of the memory is energies so it saves the power hence it is considered as a low power, it can also control both the memory at a time and it all depend in the input of chip select which is of 2 bit if it is 01 only first memory will be activated if it 10 only second memory will be activated if it is 11 the both the memory will be activated this will be controlled by the DDR controller. Hence LPDDR4 Low Power Memory Device Standard is designed to satisfy the performance of a memory density demands.

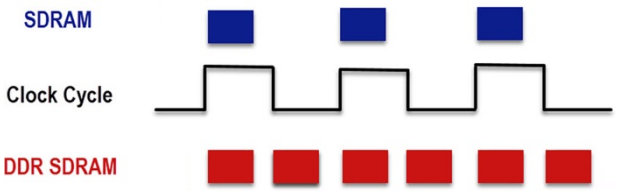

Fig 2: DDR waveform

Double data rate (DDR) memory is that it can receive or send the signals twice per clock cycle that is it works on both positive and negative clock cycle as shown in fig: 2. DDR-SDRAM, sometimes called "SDRAM II" can transfer data twice as fast as regular SDRAM chips. Hence SDRAM II is considered as faster than SDRAM.

IV. SOC DESIGN DETAILS

The LPDDR4 design hascontrol signals as a command in the bus that controls the operation of DDR interface. It is of SOC of AXI protocol, DDR controller and two DRAM memory as shown in the fig 1 LPDDR4 architecture. The memory starts chip selection operation with an activate command followed by a write or read command. The address is sent followed banks and particular byte address. There

are 16 bank in particular DRAM in each bank hexadecimal of F00F byte of registers are implemented and those kind of two set is been implemented since it is of LPDDR4 architecture and the overall it of 2MB memory size. In a single read/write operation, for each data, an address is provided. In a burst write operation, it starts writing from the user provided address that combines of bank address and the particular byte address and continues for a burst length of eight bit of data. The signals are clocked to the rising edge of the clock. The two-step process of read (RD) and write (WR) operation is taken half of the single clock cycle or the operation in done is positive edge or negative edge of clock cycle. An activate command (ACT) opens a row in a bank and makes it accessible for succeeding write (WR) and read (RD) operations. The activate command selects the bank, bank group, and row to be activated. This step is called RAS (Row Address Strobe). The step CAS (Column Address Strobe) accounts the registered address bits and concides it with RD or WR command. The DDR controller will monitor the commands of states which includes preselect, precharge, no operation, refresh, activate, and mode register set commands. The precharge (PRE) command de-activates a current open row. The de-activating of open rows can be done automatically after a write or read operation is complete using write with auto precharge (WRA) and read with auto precharge (RDA).

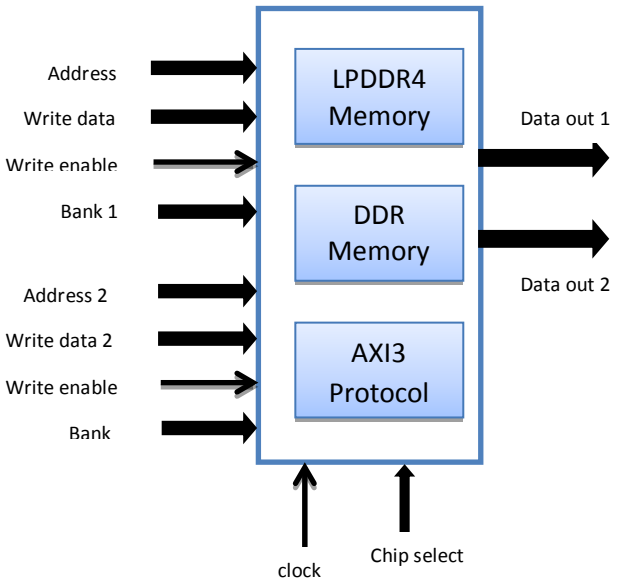

Fig 3: SoC top module

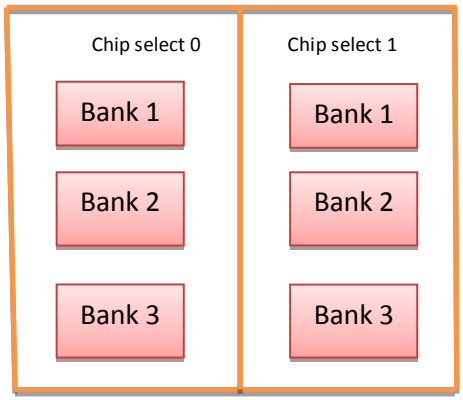

Fig 4: LPDDR4 structure

V. RESULTS AND DISCUSSION

The design has been implemented with veriloghardware description language. The formal verification for each and every block are written in testbench and is simulated with the help of the Xilinx 14.7 software tool and integration of all the block of the SOC verilog design is done using ModelSim 10.5 software.The RTL diagram is shown in Fig 4. The memory is tested with the help of automatic test pattern generator in the testbench. The Fig .5 and 6shows the simulation snapshots of LPDDR4 memory read write operation by AXI3protocol mechanism. The input automatic test pattern generator is fed as the input to the design and verifiedthe functionality of the design and code coverage of the complete design is verified and its report is shown in Fig 8.

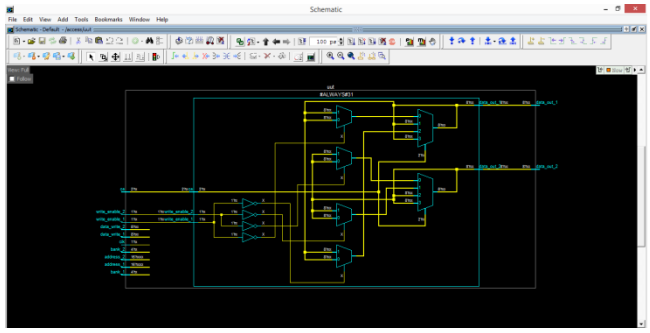

Fig 5: RTL Diagram

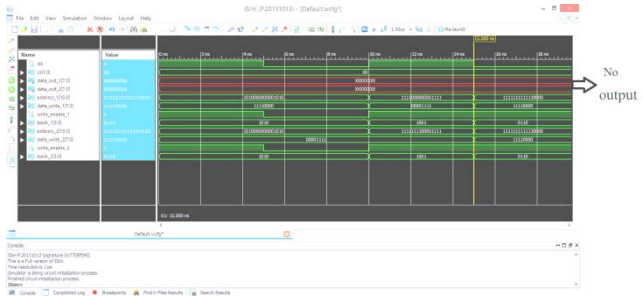

Fig 6: NO Output since CS=00

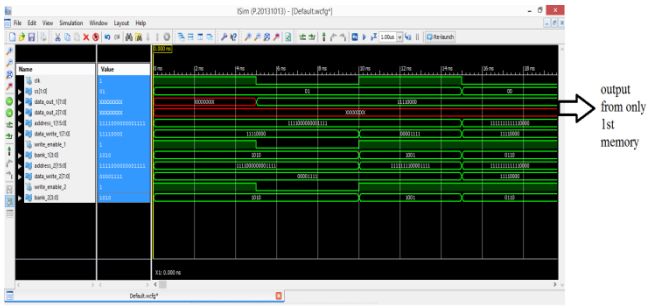

Fig 7: output on only first memory since CS=01

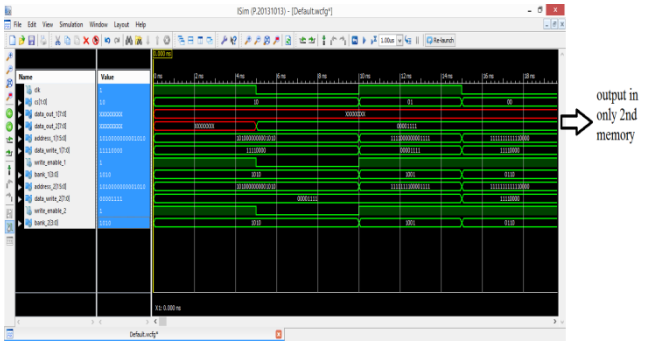

Fig 8: output on only second memory since CS=10

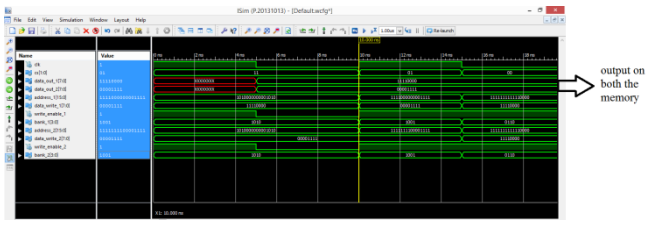

Fig 9: output on both memory since CS=11

Fig 10: Functional Coverage report

VI. CONCLUSION

The LPDDR4 memories offer higher transfer rates at the half clock cycle.The LPDDR4 architecture is of operating a dual DRAM if only one DRAM is using the other will be completely off hence it is more power saving, the throughput of high speed memory interface withthe AXI3 protocol becomes a high speed in data transfer of a memory design. Despite the limitations in hardware functionality, we have enhanced the throughput efficiency from DDR controller interface and handshaking mechanisms. Hence such design is required to handle high speed interfaces compromising the reliability of the data In future, this design could be extended to the Network on Chip (NoC) Architectures to achieve greater throughputs in the field of storage area networking (SAN).

REFERENCES

[1] AbhinavTiwari, Jagdish “Nagar An Efficient AXI Read and Write Channel for Memory Interface in System-on-Chip” International Journal of Digital Application & Contemporary research Website: www.ijdacr.com (Volume 3, Issue 3, October 2014)

[2] Payal M J1, R N Awale2 “CASE STUDY OF LPDDR4-PHY” International Journal of Recent Trends in Engineering & Research (IJRTER) Volume 03, Issue 06; June - 2017 [ISSN: 2455-1457]DOI : 10.23883/IJRTER.2017.3298.PATA4A

[3] Sarojini C, JaisinghThangaraj “Implementation and optimization of throughput in high speed memory interface using AXI protocol” IEEE - 43488

[4] Vijaykumar, R K Karunavathi, Vijay Prakash, “Design of Low Power Double Data Rate 3 Memory Controller with AXI compliant”, International Journal of Engineering and Advanced Technology (IJEAT), ISSN: 2249 – 8958, Volume 1, Issue 5, June 2012.

[5] Osborne, S., Erdogan, A.T. Arslan, T., Robinson, D., “Bus encoding architecture for low- power implementation of an AMBA-based SoC platform”, IEEE Proceedings on Computers and Digital Techniques, Vol. 149, Issue 4, July 2002.

[6] Fu-ming Xiao, Dong-sheng Li, Gao-Ming Du, Yu-kun Song, “Design of AXI bus based MPSoC on FPGA”, 3rd International Conference on Anti-counterfeiting, Security, and Identification in Communication (ASID), 2009.

[7] Sánchez-Peña, A., Carballo, P. P., García, L., &Núñez, A., “VIPACES, Verification Interface Primitives for the Development of AXI Compliant Elements and Systems”, IEEE 9th EUROMICRO Conference on Digital System Design: Architectures, Methods and Tools, 2006.

[8] Ashwin K. Kumaraswamy , V. A. Chouliaras , T. R. Jacobs, J. L. Nunez-yanez, “System-on-Chip

Design Framework (SDF) unifying Specification Capture and Design Modeling", In Proceedings of the 2005 Electronic Design Processes (EDP) Workshop, pp. 6-8, April.

[9] Na, Sangkwon, Giwon Kim, and Chong-Min Kyung, "Lifetime maximization of video blackbox surveillance camera", IEEE International Conference on Multimedia and Expo (ICME), 2011.

[10] Na, S., Yang, S., & Kyung, C. M., "Low-power bus architecture composition for AMBA AXI", Journal of Semiconductor Technology and Science, Vol. 9, Issue 2, 2009.

BIOGRAPHIES

Gopalakrishna P Received his B.E. degree in Electrical & Electronic Engineering From M S Engineering college Bengaluru, Karnataka India in 2019. Presently pursuing in MTech.(Specialization in VLSI Design and Embedded system) from BNM institute of Technology, Bangalore, Karnataka, India from 2019-2021.

Dr. P. A. Vijaya is Presently working as an Professor and Head, Department of ECE, BNM institute of Technology Bangalore, Karnataka, India. She has 35 years of teaching experience. Her areas of interest are Digital system design, Embedded systems and Sensors.