Novel Approach to Measure Internal Power Domain PG Route Weakness

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Abstract:—*Grid weakness measurement is an extremely important process in modern day VLSI design flow. In designs that contain power gating switches, there are additional challenges. It is desirable to find the PG grid weakness of only the gated domain. The tools used in industry typically measure the total voltage drops from bump location to the transistor pin. This voltage drop is the summation of the voltage drops in external domain, switch pin network and internal domain. This paper explores the ways to measure the internal pin domain voltage exclusively. Ansys Totem tool is used for simulation. Finally, the simulation results are presented to propose the effectiveness and accuracy of the givensolution.*

Index Terms— Ansys Totem, Dynamic Analysis, Node Voltage Measurement, PG Grid Weakness, Power Gating, Gated Domain, Transistor Pin Voltage

1. Introduction

Low power design is an extremely important constraint for nanometer designs today. The market forconsumerand wireless devices is rapidly changing, driven by the convergence of applications, standards, and usage. Complexity challenges are forcing these devices to be designed at 90nm and below geometries where transistor leakage is increasing exponentially. For these devices to deliver additional functionality without compromising on form factor or battery life, they need to employ aggressive leakage power reduction (>20X). Logic modules must be shut down when they arenot required in operation. Power gating is emerging as the techniquetoaddressthiscomplexchallenge.

Power gating is a technique used in integrated circuit designto reduce power consumption, by shutting off the current toblocks of the circuit that are not in use as shown in figure 1.

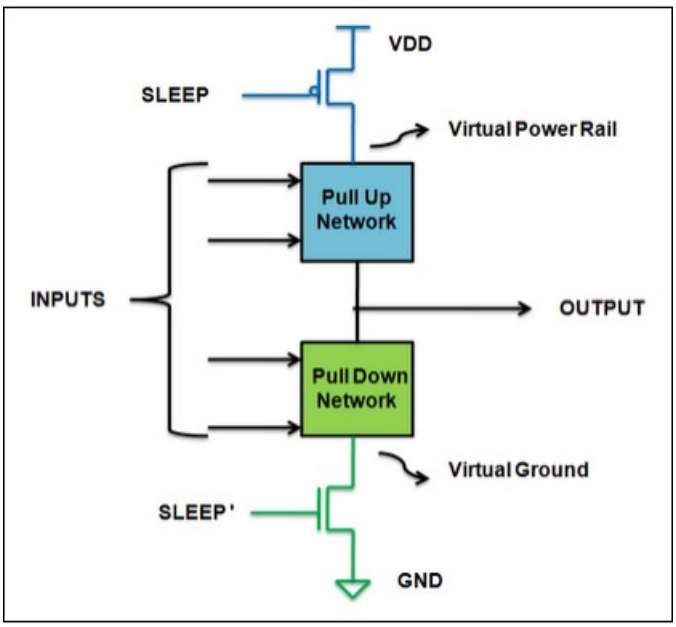

Figure 1: Power Gating Network

The switches are made of high VT transistors for minimalsub-threshold leakage. The major advantage of power gating is that the leakage power is reduced considerably. In a typical design, there are typically multiple power switches that are connected as shown in figure 2.

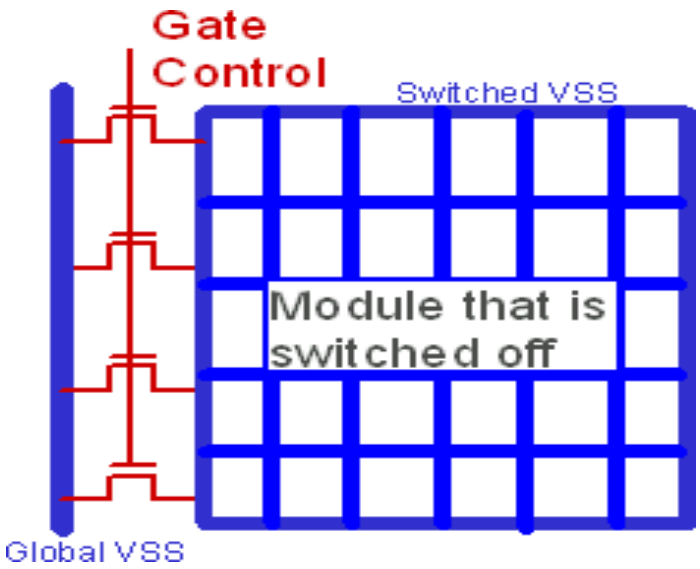

Figure 2: Multiple Power Gates

Ansys Totem is a transistor level PNR analysis platform that enables comprehensive power integrity analysis on analog mixed signal IP and full custom. Totem has application from early IC prototyping stage to system level. Early analysis enables cheaper and more impactful optimizations than are possible atsign-off.

Ansys Totem provides for different analysis like static, dynamic and signal Electromigration (EM) which helps the designer catch any gross or localized issues in power grid routing [1].

Totem currently dumps out the voltage drop from pad location to pin. However, currently, the procedure to estimate the drop from switch instances to gated domain pins, which would enable the power grid debug in internal domain is not well documented in literature. The methodology to measure the power drop from switch network to the gated domain pin is discussed in further sections and results are discussed subsequently.

2. Literature Review

The work “Power Reduction in Logic Circuits Using Power Gating for Deep Sub-Micron CMOS VLSI” discusses the importance of power gating for low power designs [2]. The impact of curbing the sub-threshold leakage due to power gating is explored in this paper.

The work “Power Grid Analysis in VLSI design” by K Shah presents the challenges arising due to increase in power on PG grid design and analysis [3]. The challenges due to the decreasing feature size is also explored in the work. It also presents the differentiates the two main analysis – static and dynamic and provides an overview of the node voltage measurement procedure. The work “Power Distribution Networks in High Speed Integrated Circuits” by Andrey V. Mezhiba and Eby G. Friedman also provides a detailed reference on power grid routing [4].

The work “Investigation of Inductance Effects Reduction in IR Drop Analysis Using Diagonal Power Routing in Power Grid Circuits in VLSI” by M.L.N Acharyulu, N.S Murthysarma and K Lal Kishore gives a novel technique to measure the voltage drop along power and ground rails[5]. This paper also takes in the inductance effects as they cannot be ignored for smaller feature size.

However, the procedure to find out the weakness in gated domain is not clearly established in literature. The methodology is discussed in the next section.

3. Methodology

The voltage drop at the transistor pin exclusive to internal domain is due to the resistance grid as shown in figure 3.

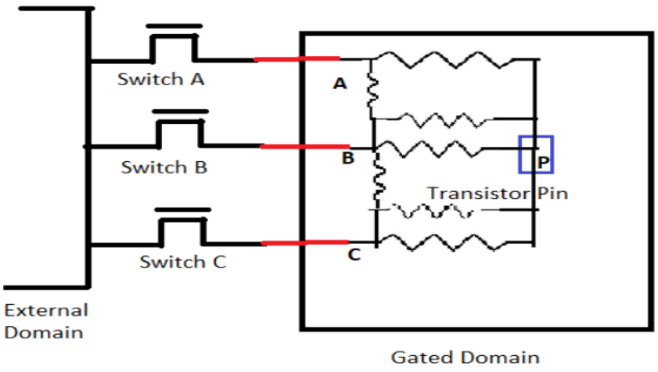

Figure 3: Simplistic View of a Gated Domain Resistance Network

The switch MOSFET gates are connected but not shown in the figure above to make the diagram less clumsy. It is extremely hard and computation intensive to find the potential drop from every switch pin to the internal domain transistor pin [6]. It is also a futile exercise to do so. Hence, computing the least resistance path for each transistor pin from a switch becomes meaningful for the following reason. The least resistance path is an indication of the path of highest current flow and hence, it is meaningful tocalculate the voltage drop across the two ends of the SPR trace. A typical SPT from Totem is shown in image 4.

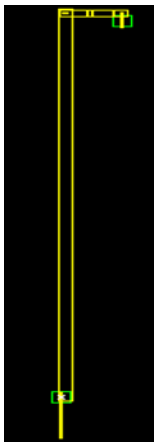

Figure 4: Sample SPR Trace

The small x indicates the switch instance, and the other end indicates the internal domain transistor pin. With SPT calculation, the switch which has most contribution to the gated pin of interest is found out.
Then, a tcl script is developed to data-mine all the said switch pin and internal pin transient voltages from Totem. Once this is done, a python script is developed to find the instantaneous voltage differences of the switch internal pin and gated domain pin. The script would report the switch-pin pairs with highest difference in sorted order. This would help the user prioritize the order in which the weakness has to be debugged.

4. Results

As stated in the previous section, to find the switch and internal transistor pin pair that causes has a major impact on grid weakness, the SPR trace is done. The trace report is shown in figure 5. The switch

instance and internal domain pin are clearly mentioned in the report in figure 5.

```
#########################################################################
#
# 2020 R2.2p4 RHEL6, built time: Aug 22 02:15:38 2020
# Minimum Resistance Path Report
#

*************************************************************

FROM: Switch Pin: V_gated, Switch Inst: adsU105 (16.605 21.004 Layer1 V_gated)
TO:   Pin: V_gated.gds6457, Inst: adsU1 (15.525 22.758 Layer1 V_gated)

# Point(XY)          Layer      Res(ohm)    ResDiff    Drop(mv)   DropDiff   Length(um) Width(um)  Net
(15.525     22.758)  Layer1       107.762     --         1.300      --         --         --         V_gated
(15.525     22.758)  Layer2        96.084     11.678     1.297      0.003      --         --         V_gated
(15.525     22.758)  Layer3        91.746     4.337      1.296      0.001      --         --         V_gated
(15.525     22.758)  Layer4        75.746     16.000     1.291      0.004      --         --         V_gated
(15.525     22.842)  Layer4        74.734     1.013      1.291      0.0002384  0.084      0.040      V_gated
(15.525     22.853)  Layer5        66.734     8.000      1.287      0.004      --         --         V_gated
(16.560     22.853)  Layer5        63.287     3.447      1.258      0.029      1.035      0.114      V_gated
(16.560     22.853)  Layer6        59.287     4.000      1.256      0.002      --         --         V_gated
(16.560     21.003)  Layer6        54.796     4.491      1.434      -0.178     1.850      0.150      V_gated
(16.605     21.003)  Layer5        50.796     4.000      1.346      0.087      --         --         V_gated
(16.605     21.004)  Layer4        38.796     12.000     1.285      0.061      --         --         V_gated
(16.605     21.004)  Layer3        22.796     16.000     1.252      0.033      --         --         V_gated
(16.605     21.004)  Layer2        16.487     6.309      1.239      0.013      --         --         V_gated
(16.605     21.004)  Layer1        0.000      16.487     1.203      0.036      --         --         V_gated

FROM: Switch Pin: V_gated, Switch Inst: adsU105 (16.605 21.004 Layer1 V_gated)
TO:   Pin: V_gated.gds6459, Inst: adsU1 (15.345 22.758 Layer1 V_gated)

# Point(XY)          Layer      Res(ohm)    ResDiff    Drop(mv)   DropDiff   Length(um) Width(um)  Net
(15.345     22.758)  Layer1       108.362     --         1.308      --         --         --         V_gated
(15.345     22.758)  Layer2        96.683     11.678     1.305      0.003      --         --         V_gated
```

Figure 5:SPR Report File

The pin switch pin voltage is shown in figure 6 and the instance pin voltage is shown in figure 7.

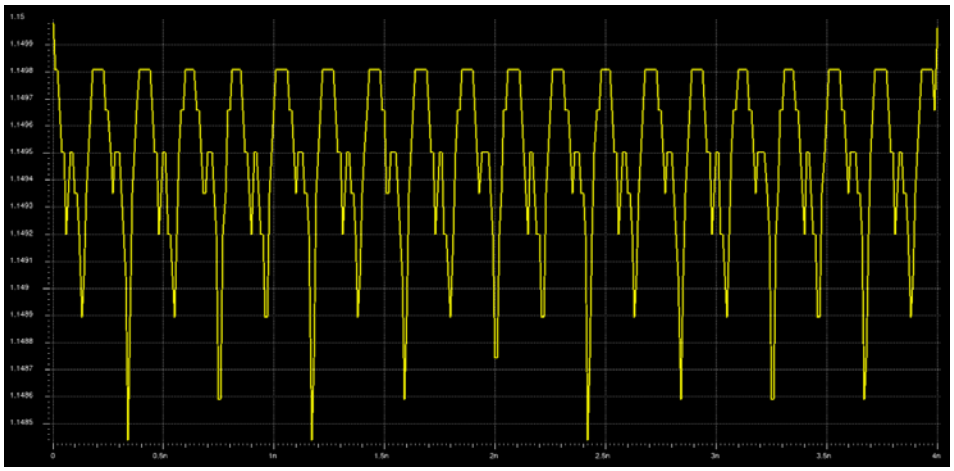

Figure 6: Switch Pin Voltage

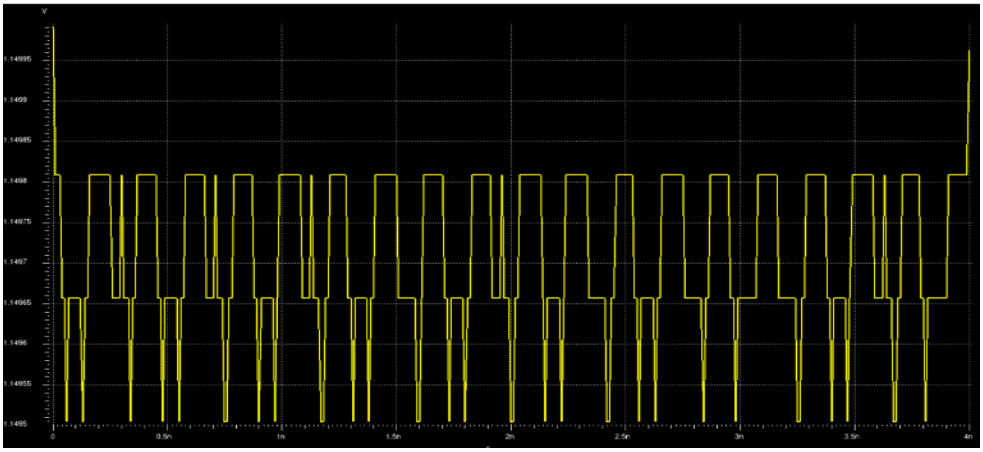

Figure 7:Internal Domain PinVoltage

The instantaneous difference is shown in figure 8. Figure 9 shows the list of worst switch pin-internal pin drops. This suggests the order in which the power grid weakness must be debugged to the designer.

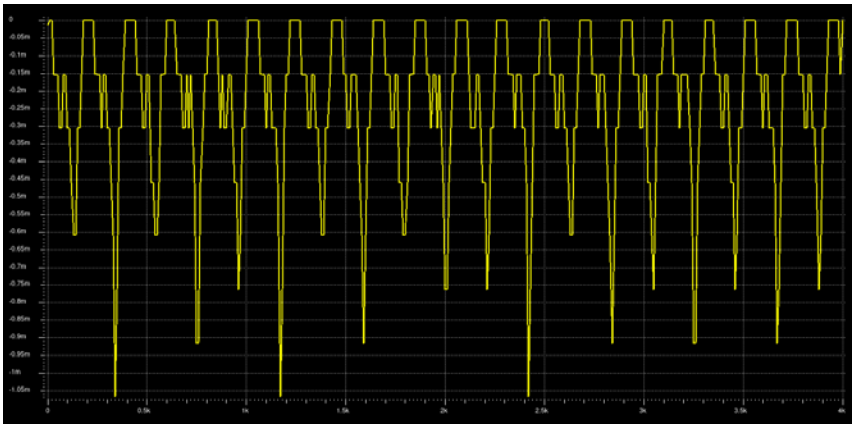

Figure 8: Voltage Drop Between Switch and Gated Domain Pin

#internal_domain_pin	switch_inst	max_diff	max_diff_time	min_diff	min_diff_time
V_gated.gds3699	adsU315	0.0010679960250854492	340.0	2.0328790734103208e-20	10.0
V_gated.gds3692	adsU255	0.0010679960250854492	1590.0	1.2555061157382141e-16	4000.0
V_gated.gds3691	adsU255	0.0010679960250854492	1590.0	1.2555061157382141e-16	4000.0
V_gated.gds3687	adsU255	0.0010679960250854492	1590.0	1.2555061157382141e-16	4000.0
V_gated.gds3648	adsU355	0.0010679960250854492	1170.0	0.0001519918441772461	1950.0
V_gated.gds3643	adsU355	0.0009150505065917969	340.0	0.0001519918441772461	1950.0
V_gated.gds7378	adsU283	0.0004580020904541016	1570.0	0.0	30.0
V_gated.gds6461	adsU105	0.00015306472778320312	230.0	8.131516293641283e-20	10.0
V_gated.gds6459	adsU105	0.00015306472778320312	230.0	8.131516293641283e-20	10.0
V_gated.gds6457	adsU105	0.00015306472778320312	230.0	8.131516293641283e-20	10.0

Figure 9: List of Worst Instantaneous Switch – Pin Drops

5. Conclusion

The procedure to quantitate the gated domain weakness by measuring the worst switch to internal pin voltage drop was demonstrated in this paper. This was achieved through various scripts to data-mine transient voltages from Ansys Totem and comparing the instantaneous voltage differences. This approach gives a more realistic idea of the drop when compared to the voltage drops mentioned in SPR report as this approach considers instantaneous drop as opposed to SPR which considers peak drop at each node. This procedure helps the designer prioritize the order in which debug must be carried out.

REFERENCES

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