Non-Destructive Vector Fault Locator to Detect Resistive Open Defects in Static Random Access Memory with Improved Performance

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Abstract. *The efforts in the semiconductor industry lead to the up-gradation of device size and performance of the devices. Extensive use of cache memory with significant size has become the requirement of most devices, applications and gadgets. Advanced nanotechnology has resulted in scaled devices and more components with complex circuitry on system-on-chip. The memories are placed incredibly more profound in the die, and memory pins are not accessible readily, leading to more complications in testing the memories. The manufacturing of scaled devices is also a challenging task. A slight variation in doping concentration or process, supply voltage, temperature variations leads to faults in the memory. Advanced technology has increased the possibilities of occurrences of resistive defects in memories. For the smooth operation of systems with high reliability, it is essential to detect all the defects in the memory. In this paper, the detection of resistive defects is proposed at an early stage to increase the life span of the memory cells. Feeble cell detected at an early stage inhibits the more mutilation of the cells and improves memory reliability. An extensive range of defective values is used to analyze the proposed method to cover all positions of the defects in the cell. The proposed method detects the resistive defects with a minimum test time of 81.95µs for 4KB of the memory and contributes a negligible area overhead of 0.77%.*

Keywords: Cache memory, faults, SRAM, resistive defects, test time

1. Introduction

As technology has advanced in the deep submicron domain, resulting in the minimum feature size. The reduced feature size has led to a higher density of memory, which is the most crucial part of the manufacturing industry and applications based on the semiconductor material. Also, memory has become one of the most inseparable parts of system-on-chip. In today's micro-miniature world, human life has become bursting with portable devices and gadgets. The maximum number of applications are now entirely dependent on the semiconductor electronics field. For such an essential part of the applications, the memory must be fault tolerant. Static Random Access Memory (SRAM) get used in many applications with different types of domains. Memory has become an imperative part of the system, testing of memory should be performed persuasively. Fast testing with less hardware is a crucial parameter for testing technology. Effective memory testing is required to affect the yield, reliability and quality of system-on-chips [1]. Earlier testing methods based on DC or AC parameters are not useful as memory pins are not readily available as memory gets embedded deeply inside the chip. Different

environmental conditions like temperature, pressure, vibrations, electromagnetic rays, power supply fluctuations, humidity etc., cause faults in the memory [2]. Minor variations in the doping concentrations during the manufacturing process may result in memory faults [3]. Process variations also cause faults in memory due to changes in channel length, oxide thickness etc. and generate instability in the device [4]. The presence of faults gives high current leads to high power dissipation, impacting the reliability of the systems and applications [5]. Encounter with various rays and radiations, aging effects also result in faults in memory. Earlier work by scientists has implied different methods for the detection of defects in memory. Deviations in the supply voltage have used to detect the faults in memory [6]. Active wordline duration has protracted for detection of defects in memory [7]. Using the active low precharge, coupling faults are detected by read equivalent stress [8]. The occurrences of the defects affect the symmetry of the SRAM cell and make the cell unstable. Using the seventh transistor in the cell, power in the conventional operation of the cell can be reduced [9]. The faults in the memory showing the characteristics of resistance expressed as resistive defects in the memory. These defects may appear at various locations in the cell. The resistive defects disturb the charging path of the node or discharging path during the conventional operations of the memory. A small difference in the ground voltages has applied for the write operation to detect the defects in memory [10]. Ensuing operations on the same cells giving higher aging effect and reducing reliability should be condensed [11]. Precharge voltage minimized to reduce the power in normal operations of the memory [12]. Earlier variations in the supply currents at both the logic levels are used to detect the faults in the memory [13]. But with advanced technology, leakage current has increased, making the prediction challenging to detect the faults. Exploration of different March tests is shown [14]. Logic fault models used for defects in the memory cell has discussed in detail [15]. Using the cell ratios and applying specific read operations generates the voltage on bitlines to detect faults [16]. Stress exerted on wordline has used to detect the defects in memory [17]. Variations in quiescent supply currents have used to detect the faults [18]. Deviations in the transient current are used for the detection of the faults at block level [19]. The detection of bridging defects is discussed [20, 21]. Defect detection by using the bias temperature instability to analyze the aging effect explored [22]. Lowered wordline voltage with varied timing circuitry method is used for detection of defects [23]. Critical testing technique with less overhead and time requirement is needed to cover a wide range of faults in memory. The remainder of the paper has organized as follows. Section 2 gives the details of the resistive open defect in the memory cell. Section 3 shows the detection of resistive defects using the proposed method. Section 4 explores the simulation results, and section 5 concludes this paper.

2 Background

SRAM is popular as cache memory due to its high-speed characteristic. The main advantage of SRAM is it does not require any refresh circuitry. The cell can hold the data indefinitely unless replaced or till the power-on. L1 and sometimes L2 level cache in the systems and applications are made of SRAM. Many researchers have proposed different topologies of SRAM cell with a varied number of transistors. Still, the conventional six transistor cell structure is more rigid, steady and symmetrical design gives good stability.

A. The structural design of SRAM cell

The SRAM cell is based on the latch type structure, made by two inverters connected in the cross-coupled with each other. The outputs of inverters are fed through as the input to

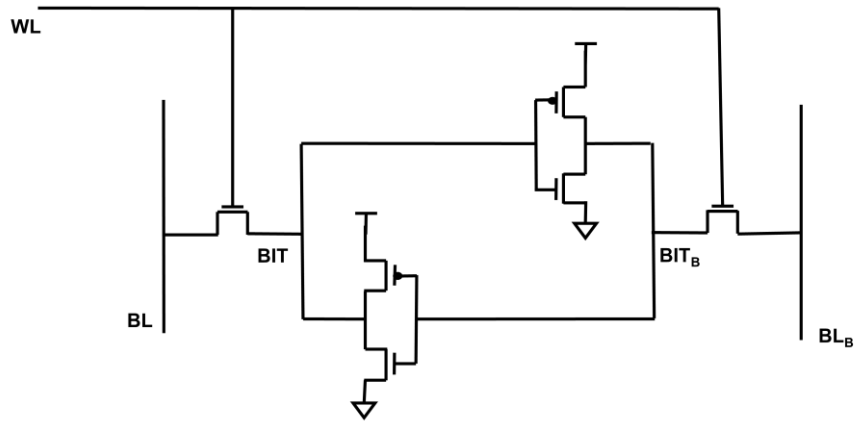

Fig. 1. The structure of SRAM cell

other inverter. The generated feedback structure supports retaining the data in the cell indefinitely without any refresh circuitry. As shown in Fig. 1, the design structure can hold 1-bit data as BIT with its complement BIT_B. The structure is symmetrical, having a set of pullup transistors, pulldown transistors and access transistors. The role of pullup transistors, which are PMOS transistors, hold the data as logic 1 at node BIT (BITB), whereas pulldown, which are NMOS transistors, hold the data logic 0 on the opposite node. The nodes are also referred to as Q and $\overline{Q}$ by different researchers. At one time, a pullup transistor in one inverter and a pulldown transistor in another is active to balance the nodes. The bitlines BL and BL_B are used for communication between the cells and other peripherals required to access the cells. With the coordination of the bitlines, data can be written onto the cells or read from the cells. The wordline WL is used to activate the cells with the help of access transistors, generally NMOS transistors. The cell structure and required peripherals such as precharge circuitry, sense amplifier etc., have designed using 45nm technology for SRAM.

B. Defects in the SRAM cell

The resistive defects in the SRAM cell may occur at different locations, as shown in Fig. 2. The defects may occur due to changes in environmental conditions like humidity, temperature, pressure, vibrations, and power supply fluctuations or process variations. The defects may also arise during the manufacturing process due to doping concentration variations. The significant locations of the defects are shown in Fig. 2 since the SRAM cell is based on symmetry, so taken as standard locations of defects [15]. The defects may occur at any one of the terminals of pullup, pulldown or access transistor. The defects disturb the nodes' regular charging or discharging path or disturb the inputs to the inverters, resulting in unbalancing the cell and a drop in the node voltage. The effect of the resistive defect on the operation of the cell depends on the defect value. For lower value range of defects up to a few kilo-ohms are called weak resistive defects, whereas higher values of defects starting from mega ohms range to higher value upto open defect are called strong resistive defect. The impact of strong resistive defects is more on the conventional operation of the cell. The logical behaviour of the cell changes due to strong defects. Sometimes due to aging effects, the strong defects may result in breakage of contacts or connections.

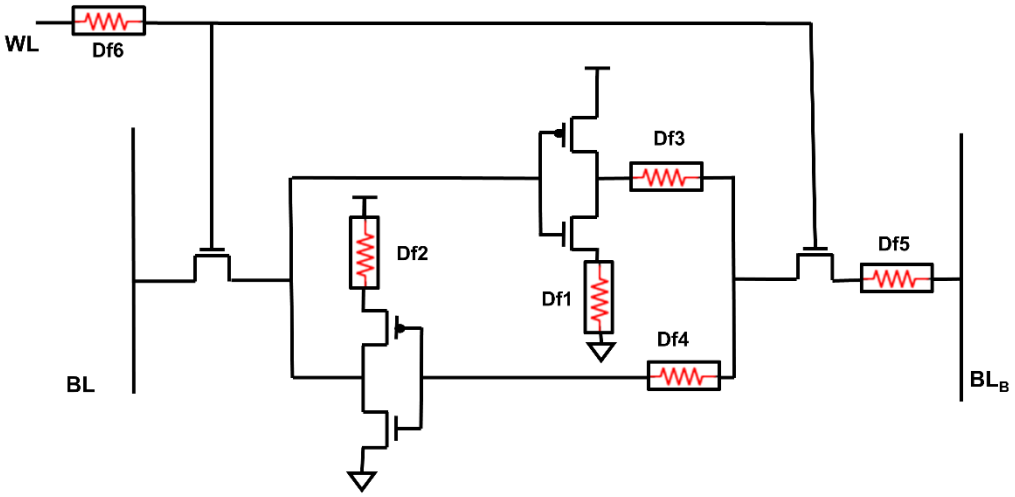

Fig. 2. Resistive open defects in SRAM cell [15]

In the SRAM cell, resistive defects may occur between any two connected terminals or the nodes of the cell. Either the defect may occur in the connecting wire or between two separate terminals called resistive bridging defects. The defects may arise in supply voltage connections, wordline connections or bitline connections. The defect Df1 present at the source terminal of the pulldown transistor disturbs the read operation of the cell by resisting the discharge path through the pulldown transistor. A higher value of the defect will decrease the voltage at node BIT and may result in the flipping of the data. The defect Df2 exists at the pullup transistor's source terminal gives resistance to the charging path of the node BIT. Since the role of the pullup transistor is to hold the logic 1 data is impacted by this defect may result in the flipping of the data since the node voltage couldn't turn on the NMOS transistor in other inverter. Hence this defect location is the primary concern in the cell since it disturbs the stability of the cell and also affects the hold operation of the cell rigorously. The defects Df3 and Df4 occur at the output and input terminals of the inverters. Hence it drops the voltage getting fed to the other inverter, node voltage and disturbs the normal operation of the cell. The defect Df5 exist at the connection between access transistor and bitline. The strong value of the defect prohibits the write operation of the cell, and the communication between the cell and other peripherals also gets affected. This type of defect gives the transition faults since the data in the cell couldn't switch from logic 0 to 1 or logic 1 to 0. The defect Df6 occurs at the wordline signal connection to the gate terminal of access transistors. The strong value of the defect makes the wordline signal unable to activate the cell. Hence read or write operation couldn't take place with the associated cell. So it is crucial to detect all these defects for the smooth operation of the cells and to improve the reliability of the memory.

3 Non-Destructive Vector Fault Locator Technique for Defect Detection

Identification of the resistive defects in the cell is crucial as it hampers the normal operation of the cell. Manifestation of the defects lowers the node voltage, results in flipping the data or disturbs the hold, read, or write operation on the cell. The SRAM cell is designed using the cell ratio of 1.5 and pullup ratio of 1.2 to give better stability using 45nm technology. The peripheral circuits, such as precharge circuit, sense amplifier, Input/Output circuit etc., are also designed and connected to the cell and simulations are performed on the cell for read and write operations. The basic principle of the proposed method is the presence of the defect generates the deviations in the node voltage, which can be reflected along the bitlines, and this difference voltage across bitlines can be sensed to detect the defects in the memory cells. The new fault detection method is proposed to detect the defects in the SRAM cell called Non-Destructive Vector Fault Locator (NDVFL), as shown in Fig. 3. In this method, the difference between the nodes BIT and BITB is sensed to detect the fault. The difference in the node voltages is made to reflect on the bitlines by activating the cell. The method is stressed for the resistive defect faults in memory. The design of the schematic of the SRAM cell and its peripherals are verified with the simulations. The basic idea is to sense the difference between the two nodes of the cell in the form of bit information stored by the cell. Due to the defect, there will be a change in voltage levels of bit information at the nodes. So this difference is detected with the help of the difference amplifier. Due to the precharge circuit, there will be the presence of residual voltage on the bitlines.

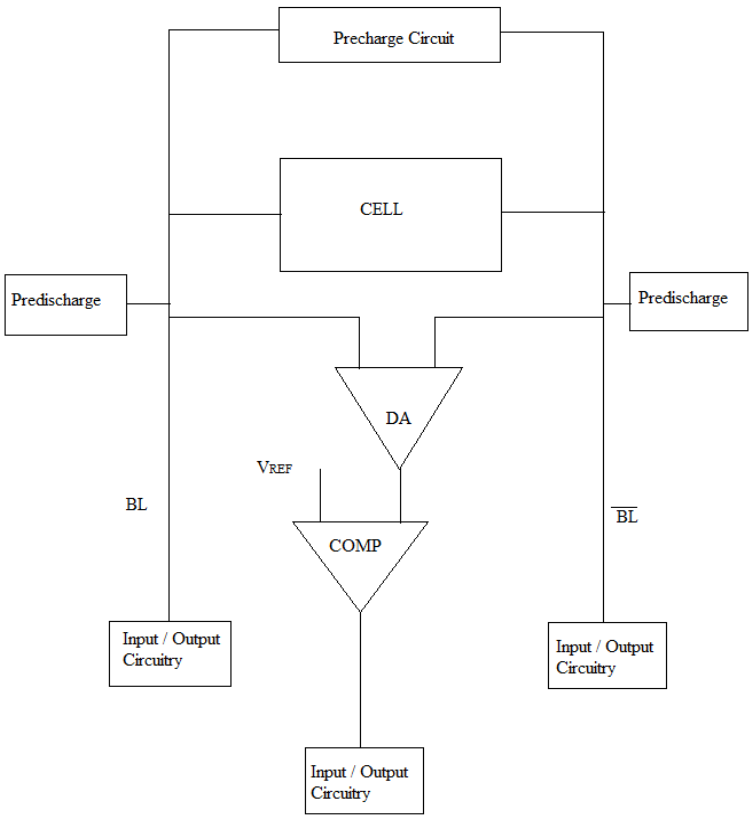

Fig. 3. Block Diagram of Proposed Defect Detection Technique

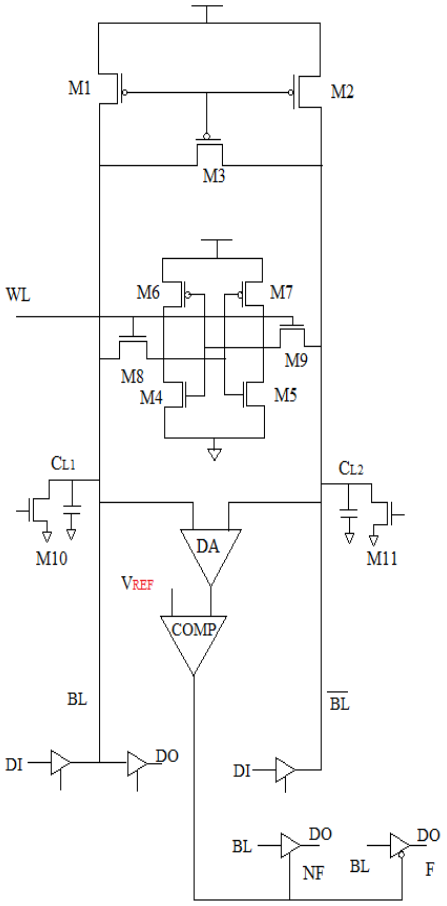

Fig. 4. Schematic Diagram of NDVFL Technique

So predischarge circuit connected to the bitlines is used to clear the bitlines before starting the fault detection. This is done with the help of NMOS transistor and parasitic capacitance present on the bitlines, as shown in Fig. 4, representing the schematic of the proposed NDVFL method. CL1 and CL2 are signifying the effective parasitic load on the bitlines. The bitlines are precharged with the help of the precharge circuit for read operations by using transistors M1 and M2. Transistor M3 is used as an equalizer to obtain equal voltages on both the bitlines. After the precharge, the structure of the six transistor cells is connected where transistors M6 and M7 are acting as pullup transistors, transistors M4 and M5 are acting as pulldown transistors, and transistor pair M8 and M9 are acting as access transistors used to activate the cell through the wordline signal WL. If the data stored in the cell is logic 0, then transistor pairs M4 and M7 are active to hold the data at BIT as logic 0 and its complement as logic 1 at the opposite node.

For logic 1 data storage, the transistors M6 and M5 are active, making the node BIT as logic 1 and BIT_B as logic 0. With the help of a wordline signal, the cell is activated for conventional operations. Then, the data stored in the cell gets connected to the bitlines. Hence, one node gets discharged through a pulldown transistor with logic 0 voltage stored, and the opposite node doesn't change, which creates the voltage difference across the bitlines fed to the sense amplifier to give strong data to the Input/Output circuit. After the read operation gets over, the residual of the precharge voltage remains on the bitlines, which doesn't allow to get perfect voltage levels of the nodes on the bitlines for the

defection of faults. Hence a predischarge circuit is connected by using transistors M10 and M11. These transistors are activated to discharge the bitlines totally for the residual charge present on the parasitic capacitors along the bitlines. Hence bitlines become neutral to get the node voltages correctly on bitlines after activating the cell to detect the defects. The difference between these bitlines is sensed with the help of a differential amplifier, as shown. This difference is then given to the comparator. The difference is then compared with the reference voltage using a comparator circuit. The reference voltage is chosen as a threshold for fault detection. The output of the comparator shows whether there is a fault in the current cell or the cell is fault-free. The output of the comparator is given to the Input/Output circuitry. With this method the exact cell in the column can be detected as to whether it contains a fault.

4 Simulation Results

Initially, the design of SRAM is performed at the schematic level after testing the integrated circuit of the cell with peripheral circuitry. Later the column is designed by increasing the number of cells followed by extending the memory at byte level structure. The design of 1KB SRAM is performed using the Cadence virtuoso tool. An exhaustive number of read and write operations are performed on the cells to test the stability of the cell. Assertion of the signals for different peripherals and cell are performed to get better performance. The design is also carried out at the layout level to observe the effect of parasitic components on the conventional operation of the memory. The impact of read and write operations are also confirmed on the surrounded cells. The proposed defect detection technique is then introduced at each column of the designed SRAM. The resistive defects are introduced at different locations in the memory at a random level. At first, the one defect is introduced in the cell at one time, and its value is changed over a wide range to analyze the effect of the defect location and its value on the normal operation of the cell. Also, the minimum detectable value for each location is also observed. For lower defect values, it is observed that there is less change in the node voltage, which doesn't affect much the normal operation of the cell. But the higher defect values gives rise to higher voltage drop at the nodes, which can be detected easily by the detection circuit to indicate the associated cell is faulty. Fig. 5 shows the effect of resistive defect values on the bitline voltage, which is reflected from the node voltage by activating the defected cell.

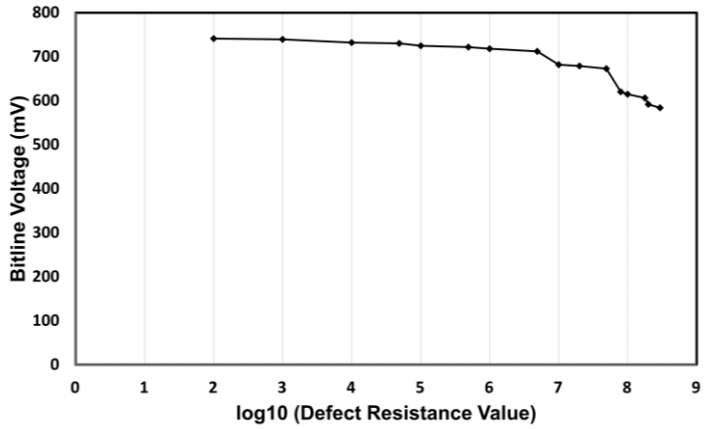

Fig. 5. Bitline Voltage against Resistive Defect Value

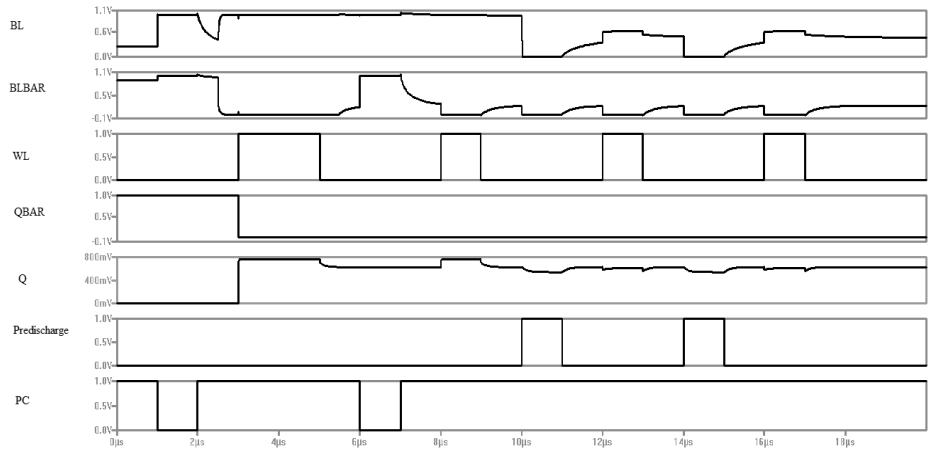

Fig. 6. Simulation Results for 100KΩ Resistive Defect

The simulation result for 100KΩ resistive defect is shown in Fig. 6. It is observed that the change in node voltages is more for the higher resistive defect, which is also getting reflected onto the bitlines. For lesser values of resistive defects, it doesn't impact more on the normal operation of the cell. The behaviour of defects changes with their values and position and resembles different logical fault models. But higher values of the defects may result in data retention fault or transition fault or may result in the flipping of the data in the cell depending on the position of the defect. In the data retention fault, the cell cannot retain the data as the resistive defect prohibits the node from getting it charged to full voltage. Hence, slowly the node voltage drops and the data may get flipped during conventional operations. A write operation on the cell couldn't be performed in transition fault, and data couldn't switch to opposite logic value. In stuck-at faults, data get stuck at logic 0 or 1 due to accidental shorts in the circuit or generated resistive defects as an unwanted connection of lower value. In the write failure fault model, the write operation couldn't take place successfully. In read destructive fault, read operation couldn't take place properly, stored data get flipped during the read operation, and available at the output. In deceptive read destructive fault, data internally get flipped, but the output shows original data. In dynamic read destructive faults, the data inside the cell get flipped after performing a write operation followed by multiple read operations. In incorrect read fault, read operation couldn't ensue properly. The defect associated with the pullup transistor is responsible for the data retention fault. The resistive defects near the bitline and wordline and the defects occur at the input/output terminal may result in the transition fault. The resistive defects associated with pulldown transistors gives rise to the flipping of the data stored in the cell or stuck at 1 fault. These defects may also result in the read destructive fault, dynamic read destructive fault or deceptive read destructive fault model.
For the analysis of the proposed method, defects are introduced randomly in the memory. The bitlines are made neutral with the predischarge circuit. For the defective cell, there is a significant voltage drop at node voltage replicated on bitline. The difference in the bitline voltage is sensed by the difference amplifier, and the data is processed and given to the comparator. The voltage is compared with the reference voltage, and if it founds below the reference voltage, it indicates that the cell is faulty. A gate circuitry is added at each column level and data on bitline is fed through the latch circuit after amplified to enhance the defect detection. They compare the logic levels before and after conventional operations to find whether the cell is defective or defect-free. The data is latched before

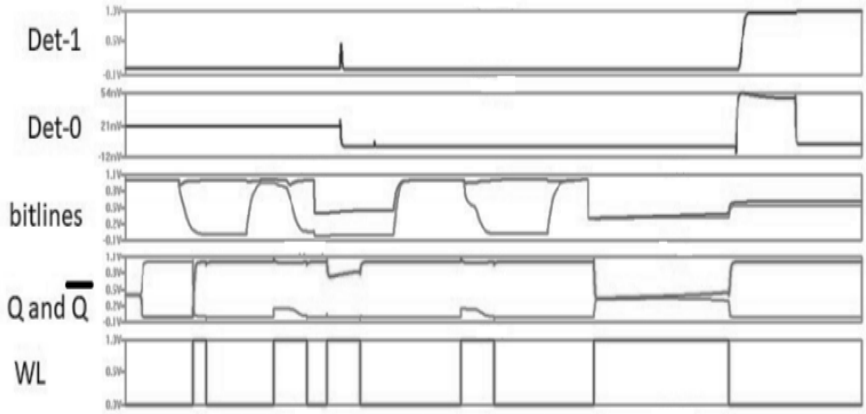

Fig. 7. Detection of Resistive Defect Df1 in the cell

write and after write for the comparison. Also, the read operation goes through the same steps. The output of the defect detection circuit is indicated by Det-0 and Det-1, as shown in Fig. 7 for simulation of the detection of Df1 resistive defect location introduced at the source of pulldown transistor. The bitlines are predischarged initially, and then stress is applied with the help of a wordline signal on the cell under test. For high-value resistive defects, it's getting detected earlier by requiring a minimum stress cycle. But for lower values of resistive defect, a significant duration stress cycle is required as the defect doesn't show any logical behavior. The dynamic read destructive faults are also observed by the proposed method by making the cell undergo a write operation followed by multiple read operations. For higher defect value, data flip occurs at 2nd or 3rd read operation, but it may go beyond the 10th read cycle for lower values. Analysis of the proposed method is also carried out at the layout level. The defects are introduced at arbitrary locations in the memory, and simulations are performed to detect the defects. The proposed method can detect weak resistive defects along with strong resistive defects. Defect-free cells simulations are also performed to verify the performance of the proposed method. The resistive defects are introduced at possible locations in the cell, and simulation results are verified for all defect locations with varied values of the defects. The lowest detectable value for different defect locations in the cell by the proposed method is compared with other techniques, as shown in Table 1. The results indicate that the proposed method can detect the resistive defects at an early stage compared to the aging technique using PMOS [22] and lowering the wordline voltage method [23].

Table 1: Lowest Detectable Resistive Defects Values

Defect Location Ω	[23]	[22]	Proposed PDFCD
Df1	214K	73K	**100K**
Df2	119M	3M	**900K**
Df4	597K	120K	**123K**
Df5	86K	90K	**77K**

Table 2: Performance Parameters

Parameter	[22]	[23]	Proposed method
Test Time	0.28ms	High	81.95µs
Area Overhead	-------	High	0.77%

Analysis of the proposed method on the performance parameter basis is also performed, as shown in Table 2. For 4KB of SRAM, the proposed method requires 81.95µs of test time which is considerably lesser than other techniques. And the area overhead offered by the proposed method is negligible as compared to other techniques. So the proposed method can detect the resistive defects in the SRAM with significantly less test time and without increasing the on-chip area.

5 Conclusion

The resistive open defects at various locations in the memory cell can be detected commendably by using the proposed method. The resistive defects of lesser values and higher values are getting detected readily by using the proposed method. It helps to improve the yield of the system and increases the reliability of memory and, in turn, of the system, gadgets and applications. Analysis of the proposed method shows enhanced coverage of the defects with less hardware requirement, and the method doesn't require any extra timing circuitry. Using the proposed method, the resistive defects in 4KB of SRAM get detected with negligible hardware and significantly less test time of 81.95µs.

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