

Real Time Implementation of Video Compression Based on DWT

Dr. Pramod Kumar Naik¹, Vyasraj T², Ramachandra Ballary³

¹ Shell India Pvt Ltd, Bangalore, Karnataka, India,

² Assistant Professor, Dept of ECE, BNMIT, Bengaluru, VTU, Belagavi Karnataka India.

³ TCE department, BMS College of Engineering, Bengaluru, Karnataka India.

¹ Pramod-Kumar.Naik@shell.com, ² vyasraj.t@gmail.com,

³ ballaryrama@gmail.com

Abstract: In this paper highly efficient 3D Discrete Wavelet Transform architecture is designed and implemented on seven series FPGA. The throughput is analyzed and its performance matrices are compared with different video file format. Today top of the line high-end image and video consume huge amount of memory. The designed architecture of DWT based video compression is again executed in parallel processing mode and its execution time is tabulated demonstrates reduced the processing or execution time. This paper demonstrates the superiority of the designed architecture both in normal mode of execution and parallel processing mode of execution. We know that higher the throughput of the video processing design results in Low power consumption. The Internal Architecture of the design is explained in brief and is synthesized in Xilinx Vivado 17.4 and implemented on Zed board. Based on the experimental results of the design being implemented on FPGA, demonstrates the memory saving capabilities and superiority of this architecture. The resultant architecture has drastically reduced latency and has enhanced the speed of operation.

Keywords- Wavelet, VLSI, Parallel Processing

1. Introduction

The extensive use of various types of multimedia devices has made video compression architecture a major research area. The significance of DWT based video compression technique is that it is widely used in major application area like live video broadcasting, video conferencing, Medical resonance imaging, and video surveillance etc. During this process we greatly reduce the consumed memory for data storage and also save the overall bandwidth required for transmission. The need of video compression is that they require less memory size to store the recorded video for major application areas. With the advent of Multimedia technology, designers and researchers design new prominent architectures. The key features of these architectures should be less power consumption and good computing speed. The success of present day multimedia based video processing application heavily relies on under lying compression algorithms. Due to above constraints there is need for dedicated VLSI based video compression architectures. The primary aim of video compression is to minimize the immerse amount of video data so that the video can be stored, transmitted and displayed efficiently. Video compression is widely used in real time, robotic operations and medical imaging. In this work we have chosen DWT based video compression architecture as its better its performance is better compared to that of DCT architecture. The computation speed of DWT is faster than other wavelet. At the same time easy to implement and consumes less computational time and resources for processing the video.

2. Proposed Architecture

The objective is to design and implement an efficient DWT processor for high end video and multimedia processing applications. Generally the digital video processing application approximately requires image resolution of 2K with data rate of 2.1 GigaBit/sec. But the processing of real time video at this work rate is beyond the scope of present date general purpose processors. At the same time the DSP processors and ASICS are very costly and are not economical. Hence an Field Programmable Gate Array (FPGA) based approach as shown in the figure1.1 is followed. Since FPGA do not have huge amount of memory which they can allocate it for huge amount data present in video processing. The DWT processing unit is provided with a splitting unit which is helps in row processing and column processing of video. 3D lifting based discrete wavelet transform architecture uses memories for spatial and temporal processing. The memory requirement dominates the performance, efficiency and cost of implementation of the design. Inside the DWT processing unit we have the combination of spatial processing unit and temporal processing unit. Spatial processing unit require N^2+8N memory and temporal processing unit require $3N^2$ memory. In DWT based video processing we perform operations on the frames of the input video. Thus we perform row and column wise processing as shown in the figure 1.1.

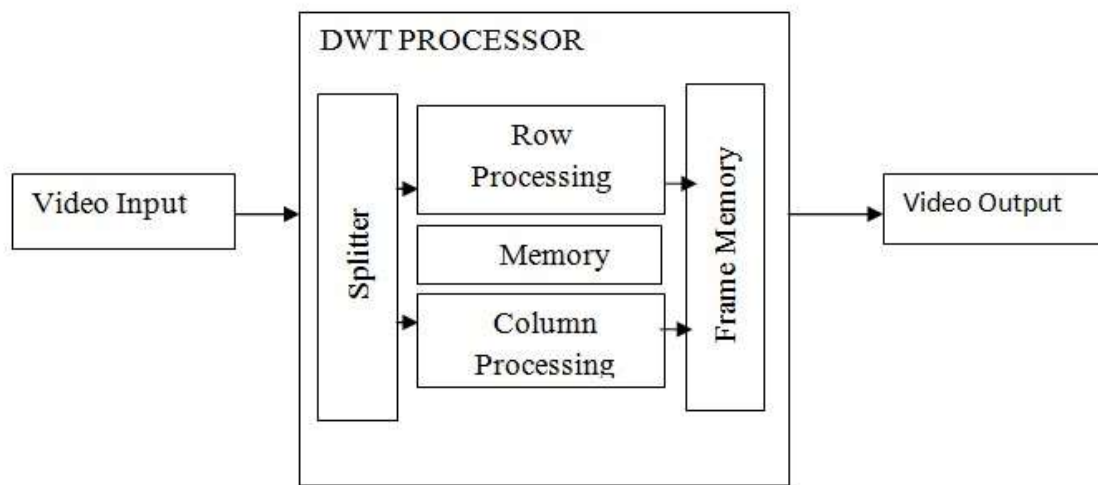


Figure1.1 Reconfigured DWT Processing Unit

3. Real Time DWT Video Compression

As a first level of decomposition this scheme in its second stage uses 2-D Discrete Wavelet Transform. Spatial domain pixels are converted into frequency domain information represented in multiple sub-bands representing different time scale and frequency points using DWT. The original image divides into four number of decomposition levels LL, HL, LH, and HH as shown in figure 1.2. The four frequency regions in the image are represented by four portions. LL is the low frequency decomposition level sensitive to human eyes.

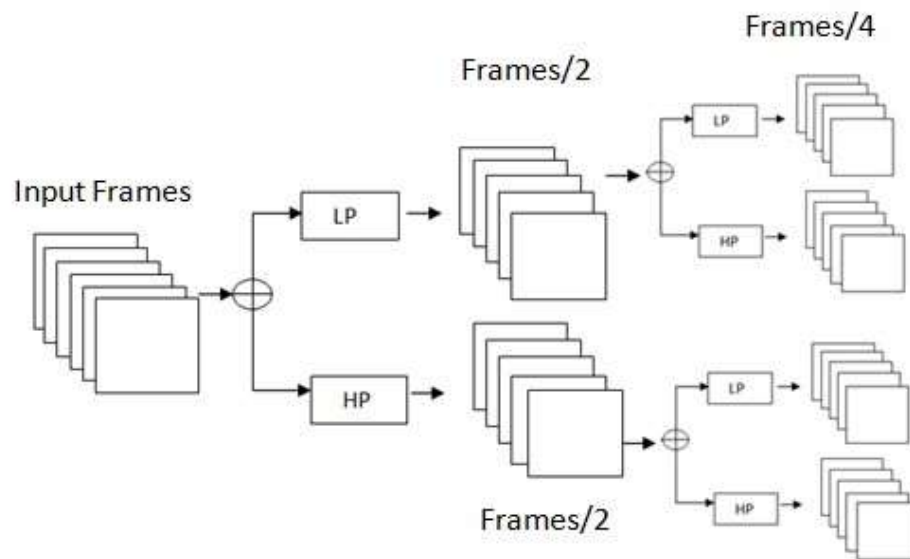


Figure 1.2 DWT based frame compression

This DWT compression technique is applied on images or on videos. But during the video compression we perform frame by frame based video compression. As shown in the figure 1.2 we apply the low pass and high pass entirely on the frame of input video. The temporal DWT as shown in the figure 1.2 applied to the frames and is called as 3D-Discrete Wavelet Transform (DWT).

4. Hardware Implementation Results

This methodology focusses on the reduction of the amount of memory available for video storage while also improving the signal to noise ratio of images obtained using the DWT algorithm over existing algorithms. Results of the system are collected on pc and are shown in frame-wise compression and video-compression manner.

The Internal Architecture of Lifting based DWT compression based architecture is designed and implemented of ZedBoard as shown in the figure 1.3 shows us the IP based DWT design and derived architecture is modeled and simulated using Vivado

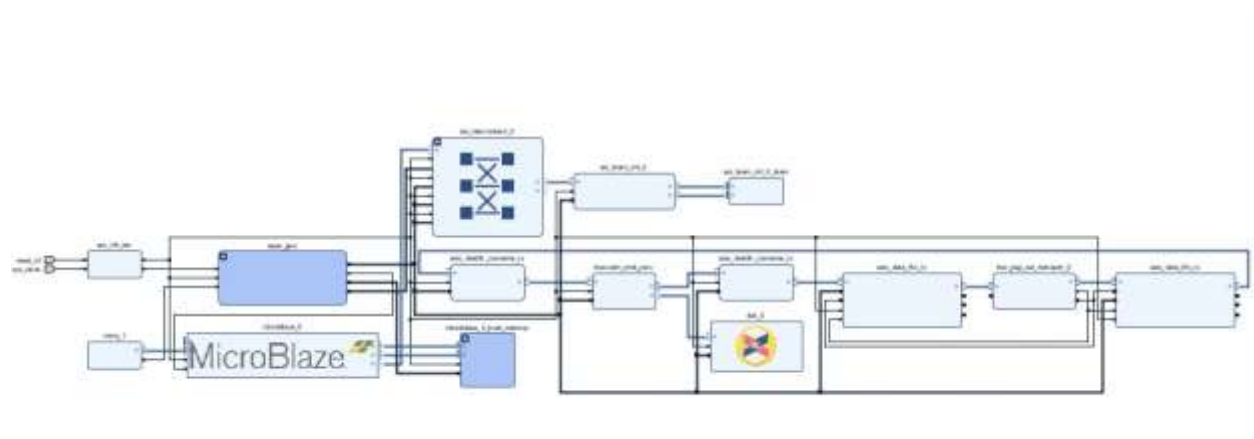


Figure 1.3 IP Based Design of DWT

Vivado 14.7 is used to synthesize the functionally verified netlist and is implemented on Zed Board. The RTL model is verified for area, power and speed. The power analysis parameters of synthesized and implemented design are listed in below Table 1.

TABLE 1: Experimental results of Power Consumption

Parameters	Synthesized Design	Implemented Design
Total On-Chip Power	1.704W	2.072W
Junction Temperature	44.7 C	51.9 C
Thermal Margin	40.3 C (3.4W)	48.1 C (3.6W)
Power Supplied to off-chip devices	0 W	0 W
Dynamic On-Chip Power	1.541 W (49%)	1.782 W (86 %)
Static On-Chip Power	0.150W (51%)	0.291 W (14 %)

5. CONCLUSION

Multiresolution presentation of images is given by the discrete wavelet transform (DWT). This work highlights on the straightforward and fast Haar implementation of DWT and IDWT algorithms using system c coding on XILINX platform. The algebraic equations of DWT algorithm are accustomed reduce the complexity and boost the computational speed. Two dimensional DWT is performed on images of various pixel size. First, the preprocessing a part of the photographs extracted from captured video is performed by using MATLAB tool. System C language-Xilinx platform is used to write the code and implemented in FPGA and the video frames that are compressed are again decompressed and using the MATLAB tool they are converted into video. System parameter like pick signal to noise ratio is measured. From the adequate simulation results we will conclude that algorithm works properly. We finish off that for obtaining higher compression, higher decomposition is required. Implementation of system using VLSI i.e. FPGA approach provides the advantages in requiring low memory requirement and consumes low power.

6. REFERENCES

- [1] Amir Said, William A. Pearlman, "A New, Fast And Efficient Image Codec Based On Set Partitioning In Hierarchical Trees", IEEE Transactions On Circuits And Systems For Video Technology, VOL-6, No.3, June 1996.
- [2] Ch. Naveen, V. R. Satpute, A. G. Keskar, K. D. Kulat, "Fast And memory Efficient 3D- DWT Based Video Encoding Techniques", Proceedings Of The International multi conference Of Engineers And Computer Scientists 2014 Vol. 1, IMECS 2014, March 12 - 14, 2014, Hong Kong, Pp.- 427-433.
- [3] Uma Sadhvi Potluri, Arjuna Madanayake, "Improved 8-Point approximate DCT For Image And Video Compression Requiring Only 14 Additions" Member IEEE Transaction On Circuit And System--1:Regular Papers, Vol. 61, NO. 6, June 2014.
- [4] B. K. Mohanty And P. K. Meher, "Memory-Efficient High-Speed Convolution-Based Generic Structure For Multilevel 2-D DWT." IEEE Transactions On Circuits And Systems For Video Technology, Vol. 23, No.2, Pp. 353-363, Feb. 2013.
- [5] Ch. Naveen, V. R. Satpute, K. D. Kulat, A. G. Keskar, "Video Encoding Techniques Based On 3D-DWT", 2014 IEEE Students' Conference On Electrical, Electronics And Computer Science, SCEECS 2014, March 1-2, 2014.
- [6] B. Das and S. Banerjee, "Low power architecture of running 3-D wavelet transform for medical imaging application," in Proc. Eng. Med. Biol. Soc./Biomed. Eng. Soc. Conf., vol. 2. 2002, pp.

1062–1063.

- [7] A. Darji, S. Shukla, S. N. Merchant And A. N. Chandorkar, "Hardware Efficient VLSI Architecture For 3-D Discrete Wavelet Transform," Proc.of 27th Int. Conf. On VLSI Design And 13th Int. Conf. On Embeddedsystems Pp. 348-352, 5-9 Jan. 2014.
- [8] K.Sureshraj, V.R.Satpute, A.G.Keskar, K.D.Kulat, "Imagecompression Using Wavelet Transform Compression Ratio And Psnrcalculations", Proceedings Of The National Conference On Computersociety And Informatics- Nccsl' 12, 23Cd&24th April 2012.
- [9] B. Das and S. Banerjee, "Data-folded architecture for running 3-D DWT using 4-tap Daubechies filters," IEE Proc. Circuits Devices Syst., vol.152, no. 1, pp. 17–24, Feb. 2005.
- [10] Chao He, Jianyu Dong, Member, IEEE, Yuan F. Zheng, Fellow,IEEE, And Zhigang Gao, " Optimal 3- D Coefficient Tree Structure For 3- D Wavelet Video Coding", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL.13, NO. 10, OCTOBER 2003, Pp.-961-972.
- [11] Anirban Das, Anindya Hazra, And Swapna Banerjee,"An Efficientarchitecture For 3- D Discrete Wavelet Transform", IEEE Transactions On Circuits And Systems For Video Technology.978-1-4799-1812-6/14/\$31.00 ©2014 IEEE
- [12] Z. Taghavi and S. Kasaei, "A memory efficient algorithm for multidimensional wavelet transform based on lifting," in Proc. IEEE Int. Conf. Acoust. Speech Signal Process. (ICASSP), vol. 6. 2003, pp. 401–404.
- [13] Nagita Mehrseresht And David Taubam, "An Efficient Content Adaptive Motion-Compensated 3D-DWT With Enhanced Spatial And Temporal Scalability", IEEE Transactions On Image Processing, VOL.15, No.6, JUNE 2006.
- [14] Ch. Naveen, V. R. Satpute, K. D. Kulat, A. G. Keskar," Comparison Of 3D- DWT Based Video Pre-Post Processing Techniques',Selected At World Congress On Engineering And Computer Science, San Francisco, USA, 22-24 October, 2014.
- [15] El Gamal And H. Eltoukhy, "CMOS Image Sensors," IEEE Circuitsdevices Mag., Vol. 21, No. 3, Pp. 6–20, May/Jun. 2005.
- [16] C. Pilrisot, M. Antonini, and M. Barlaud, "3-D scan based wavelet transform and quality control for video coding," Eur. Assoc. SignalProcess. J. Appl. Signal Process., vol. 2003, pp. 56–65, Jan. 2003.
- [17] I. Daubechies and W. Sweldens, "Factoring wavelet transforms into lifting steps," J. Fourier Anal. Appl., vol. 4, no. 3, pp. 247–269, 1998.
- [18] S. Barua, J. E. Carletta, K. A. Kotteri, and A. E. Bell, "An efficient architecture for lifting-based two-dimensional discrete wavelet transforms,"VLSI J. Integration, pp. 341–352, Jan. 2005