

# Area Efficient Modified Array Multiplier

P Akshatha Shetty

Department of ECE  
R.V. College of Engineering  
Bengaluru, India  
pakshathas.lvs20@rvce.edu.in

Dr. Kiran V

Professor Department ECE  
R.V. College of Engineering  
Bengaluru, India  
kiranv@rvce.edu.in

**Abstract** - Multipliers are widely used for various application like signal processing. Multipliers are used for multiplication two binary data. There are different kinds of multipliers with their own advantages and disadvantages.

In this paper we implemented Array multiplier which has considerably more speed but also more area, it was implemented using pseudo NMOS logic in Cadence software and the number of transistors was reduced from  $2N$  to  $N+1$  which also lead to reduction in area

**Index Terms** – Array multiplier, CMOS, Pseudo-NMOS logic.

## I. INTRODUCTION

In every known digital signal processor, a multiplier is a fundamental component they are also used ALU's, image processing.[7] Every customers would prefer faster devices with lower power usage. If the device components are faster and their size's small, will be able to reduce the power usage and performance can be eventually be increased. The multiplier takes up the majority of the space in any digital circuit. If a properly optimized multiplier is not used, it will generate lag[4]. Area, total power dissipation, and propagation latency are the most significant elements to consider when evaluating the performance of a system.

In order to meet the low-power requirements, many different approaches were suggested a few of them were Pseudo NMOS, C2MOS, Dynamic CMOS, and Domino were all used.

The shift and adds method is used by array multiplier to multiply two values. Even though it has a very regular and systematic structure, it has a big latency when the word length is long. Min C. Park et al. (1993) [1] proposed a new design based on a dual array tree structure with dual partial product arrays divided from a conventional multiplier's partial product plane. It was found that the multiplier's speed is twice that of a standard array multiplier. Despite the fact that it has a 30% larger silicon area, its architecture can be fairly compact because to its regular construction. In order to meet the low-power requirements, many different approaches were suggested a few of them were Pseudo NMOS, C2MOS, Dynamic CMOS, and Domino were all used.

In[3] it is revealed that a multiplexer-based array multiplier outperforms a modified Booth multiplier in terms of speed and power dissipation by 13 to 26 percentage due to lower internal

capacitance and how area-efficient complete adder circuits (SERF and IOT 1111) can assist reduce overall routing capacitance, leading in lower power consumption for multipliers based on these adder circuit. In[4] it introduces a new multiplexer-based truncated array multiplier that takes advantage of three existing truncation techniques and improves them. To analyse the truncation errors of the new truncated multiplier, an extensive error analysis was undertaken. In terms of latency, silicon area, and power consumption, the suggested truncated multiplier was compared to one constructed using typical truncation approaches. In[5] the different multipliers like Array multiplier, Wallace multiplier, Bypassing multiplier, Modified Booth multiplier, Vedic multiplier, and Booth recorded Wallace tree multiplier that have been proposed by many academics where compared for their performance. When comparing the various multipliers, it was discovered that the Array multiplier has the longest delay and consumes the most power, whereas the Booth encoded Wallace tree multiplier has the shortest delay and consumes the most power. While employing the partially guarded methodology, power consumption is lowered by 10-44 percent with 30-36 percent less area overhead, while using the temporal tiling method, array multiplier delay and power dissipation are observed to increase by 50 percentage and 30 percentage. The Wallace tree multiplier recorded by Booth is determined to be 67% quicker than the Wallace tree multiplier, 53% faster than the Vedic multiplier, and 22% faster than the radix 8\_booth multipliers. In[6] the series of array multipliers of different size, different delay and accuracy characteristics so one can select according to preference. In[7] the reduce multiplier power usage, a modified full adder with multiplexer is proposed. The traditional array multiplier structure is utilized to evaluate the efficiency of the proposed architecture. The designs are created in Verilog HDL, and the functionality are confirmed using Xilinx simulation. In comparison to existing techniques, the suggested multiplier's synthesis results demonstrate a 35.45 % reduction in power consumption, 40.75 percent reduction in area, and 15.65 percent reduction in delay. In[2] pseudo-NMOS was examined in a new light and discovers that SOI technology enables significant performance (speed and power) and area gains, implying that it will be widely used in the design of SOI custom-integrated circuits. As the pseudo NMOS offers advantage in terms of area[2] in this paper we use pseudo-NMOS to build array multiplier.

This paper describes the operation of pseudo-NMOS and comparison in terms of transistor for various primitive gates in section II. Then the implementation of AND, OR & XOR gates, Half adders, Full adders and array multiplier implemented using pseudo NMOS logic in section II then simulation results in section III.

### A. Pseudo-NMOS logic

Pseudo-NMOS logic with transistor count  $N+1$  the pull up network is always as compared to the CMOS there is great reduction in number of transistors. Below is the figure of inverter implemented in pseudo-NMOS. PMOS devices are good pull up resistive loads because they are fast and compact. With a fan-in, it's a pseudo-NMOS gate because each input is connected to only one transistor, the burden on the transistor is reduced prior to the gate.

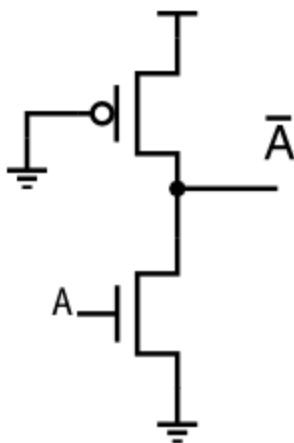


Fig. 1 Pseudo-NMOS logic

The pseudo-NMOS doesn't offer any advantage for inverter in terms of area as compared to CMOS because both have same number of transistors but other gates like AND, OR, XOR it offers advantages below is the Table which gives comparison between number of transistors in CMOS and pseudo-NMOS logic, the advantage of reduction area it comes at cost of increased static power consumption because P-MOS is always connected to supply irrespective of input.

TABLE I

COMPARISON OF NUMBER OF TRANSISTORS

Gate	CMOS	Pseudo-NMOS
Inverter	2	2
AND	4	3
OR	4	3
XOR	8	5

## II. IMPLEMENTATION

The below is figure AND, OR, XOR, Half adders all are in Pseudo-NMOS

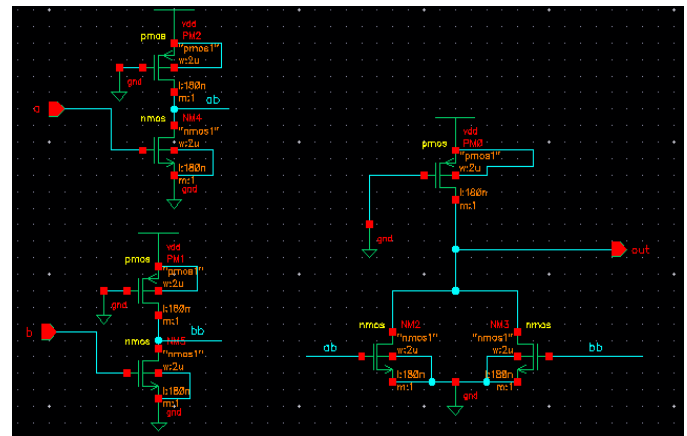


Fig.2 AND gate using Pseudo-NMOS

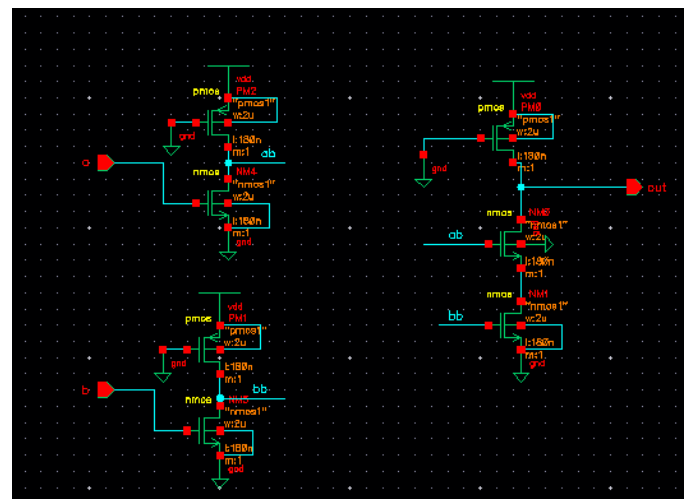


Fig.3 OR gate using Pseudo-NMOS

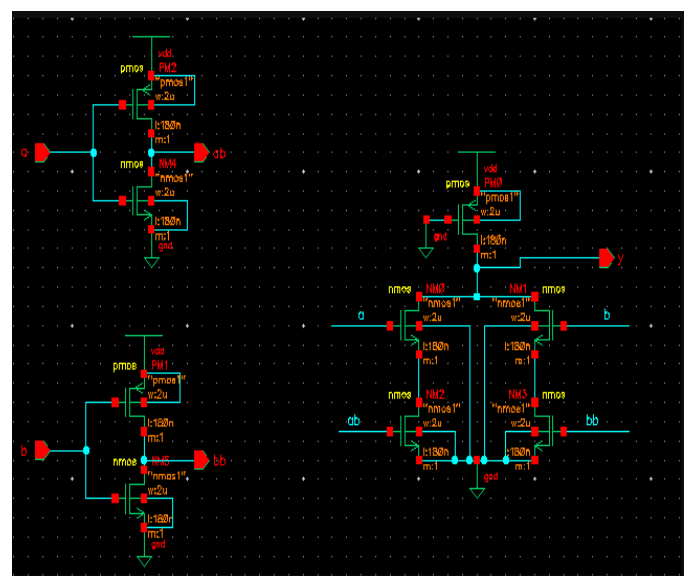


Fig.4 XOR gate using Pseudo-NMOS logic

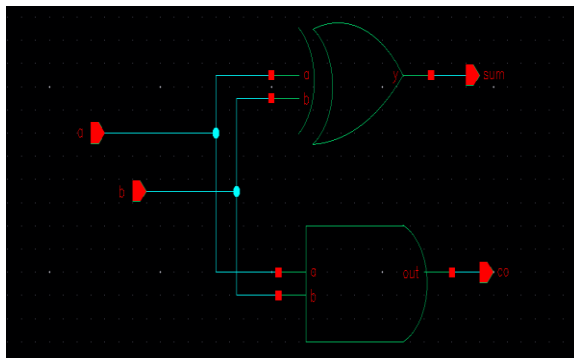


Fig5. Half adder

### A. Array Multiplier

Below is the block diagram of 4X4 array multiplier consisting of AND gate, Half adders, Full adders with 4 bit inputs and 8 bit output, in block diagram X & Y are inputs and Z taken as output. Each half adder consist of XOR gate and AND gate, array multiplier uses concept of partial product.

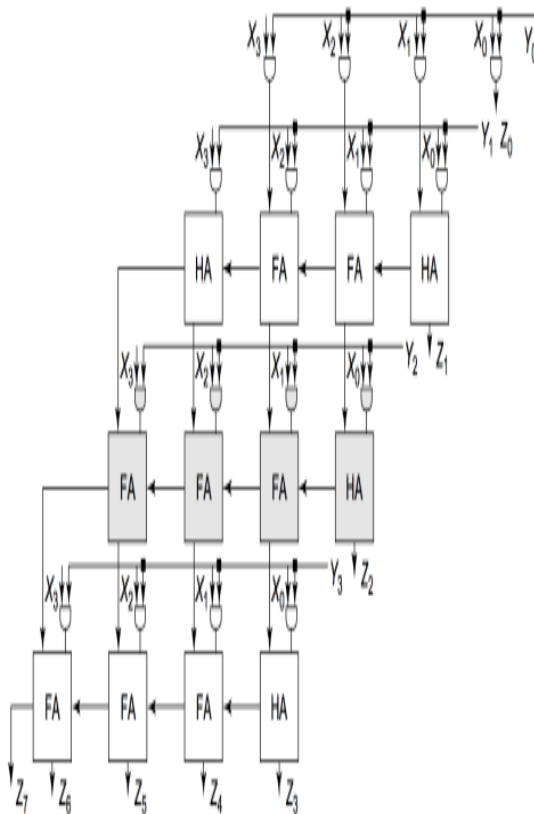


Fig.6 Block diagram of 4X4 Array multiplier

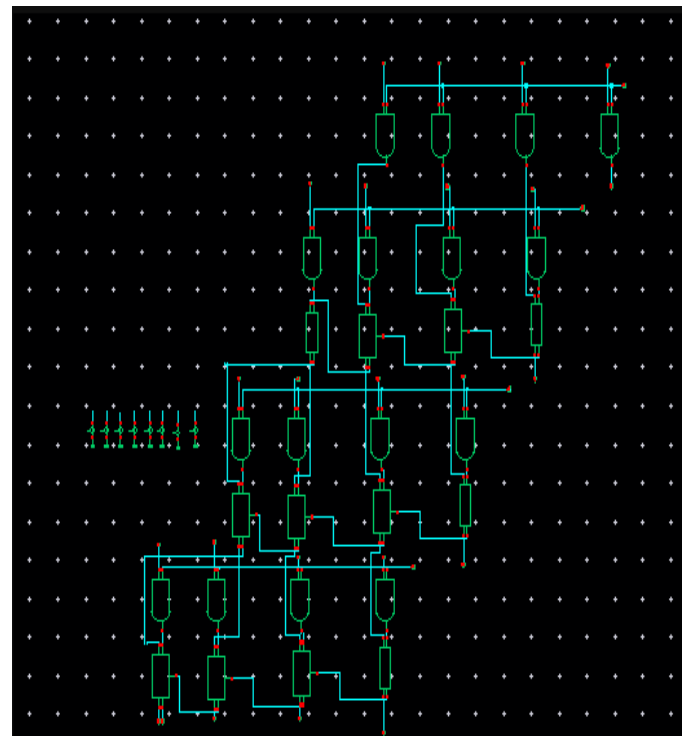


Fig7. Schematic of array multiplier

### III. Results and Conclusion

When given input as  $X=1011$  &  $Y=1101$  then the output we get  $Z=1000111$ . The array multiplier implemented with pseudo-NMOS gives an advantage over CMOS in terms of number of transistors.

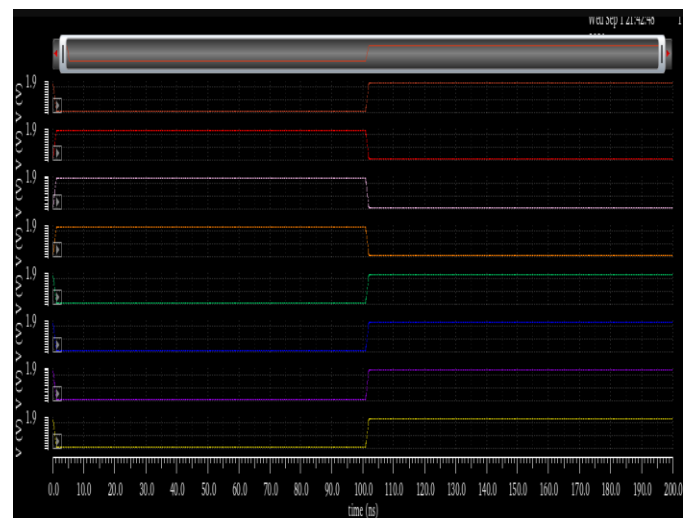


Fig8. Array multiplier output

The advantage of array multiplier implemented with pseudo-NMOS has advantage in reduction of number of transistors. If implemented with CMOS number of transistors would be 260 and when implemented with Pseudo-NMOS number of transistors are 176 and therefore there is reduction in number of area.

## REFERENCES

- [1] M. C. Park, B. W. Lee, G. M. Kim and D. H. Kim, "Compact and fast multiplier using dual array tree structure," 1993 IEEE International Symposium on Circuits and Systems, 1993, pp. 1817-1820 vol.3, doi: 10.1109/ISCAS.1993.394099.
- [2] N. Subba, A. Salman, S. Mitra, D. E. Ioannou and C. Tretz, "Pseudo-nMOS revisited: impact of SOI on low power, high speed circuit design," 2000 IEEE International SOI Conference. Proceedings (Cat. No.00CH37125), 2000, pp. 26-27, doi: 10.1109/SOI.2000.892752.
- [3] Chip-Hong Chang, R. K. Satzoda and S. Sekar, "A novel multiplexer based truncated array multiplier," 2005 IEEE International Symposium on Circuits and Systems, 2005, pp. 85-88 Vol. 1, doi: 10.1109/ISCAS.2005.1464530.
- [4] K. N. Singh and H. Tarunkumar, "A review on various multipliers designs in VLSI," 2015 Annual IEEE India Conference (INDICON), 2015, pp. 1-4, doi: 10.1109/INDICON.2015.7443420.
- [5] T. Yamamoto, I. Taniguchi, H. Tomiyama, S. Yamashita and Y. Hara-Azumi, "A systematic methodology for design and analysis of approximate array multipliers," 2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2016, pp. 352-354, doi: 10.1109/APCCAS.2016.7803973.
- [6] S. Srikanth, I. T. Banu, G. V. Priya and G. Usha, "Low power array multiplier using modified full adder," 2016 IEEE International Conference on Engineering and Technology (ICETECH), 2016, pp. 1041-1044, doi: 10.1109/ICETECH.2016.7569408.
- [7] P. Kishore, P. V. Sridevi and K. Babulu, "Low Power and High Speed Optimized 4-bit Array Multiplier Using MOD-GDI Technique," 2017 IEEE 7th International Advance Computing Conference (IACC), 2017, pp. 487-491, doi: 10.1109/IACC.2017.0106.