Comparative Review on Efficient Design of Reversible Sequential Circuits based on Optimization Parameters

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Abstraction: -Reversible computing, a well known research area in the field of computer science. One of the aims of reversible computing is to design low power digital circuits that dissipates no energy to heat. The main challenge of designing reversible circuits is to optimize the parameters which make the design costly. In this paper, we review different designs of efficient reversible sequential circuits and prepare a comparative statement based on eight optimization parameters such as Quantum Cost (QC), Delay (del), Garbage Output (GO), Constant Input (CI), Gate Level (GL), Number of Gate (NoG), Type of Gate (ToG), Hardware Complexity (HC) of Circuit.

Keywords: Reversible Computing, Sequential circuit, optimization parameters, low

1. INTRODUCTION

Computers play an important role in efficient information processing as society's productivity and economy grow. Technological advancement in the computation field continues to improve as fast as possible for our social interests. It is progressed through the improvement in the speed and power of computers. In recent year Reversible computation is considered an important way to improve the use of power of computers. Logical reversibility is the logical state of the computational device just prior to the operation (its input state) which is uniquely determined by its state just after the operation (its output state) and physical reversibility is a process that dissipates no energy to heat, and produces no entropy [1]. It is proven that each bit of information loss generates kTln2 joules of heat energy, where k is Boltzmann's constant and T is the absolute temperature at which computation is performed [2]. In reversible computation, information loss not has done during computation process due to its one to one correspondence between its inputs and outputs. It is shown that the circuit with reversible logic gates can avoid the heat dissipation [3]. The optimization of the reversible circuit is the main design issue based on different parameters which result the design costly. The most important parameters are Quantum Cost (QC), Delay (del), Garbage Output (GO), Constant Input (CI), Gate Level (GL), Number of Gate (NoG), Type of Gate (ToG), Hardware Complexity (HC) of Circuit. In this paper we review the existing works in Reversible Sequential Circuits and prepare a comparative statement based on different optimization parameters. Many researchers are involved to design new reversible sequential circuit. This paper helps them to measure the cost of their circuit and compare with other design to find the optimization of their circuit. The paper is arranged as follows: section 2 provides the description of Reversible sequential circuit and its design issues. Section 3 provides the description about the optimization parameters. Section 4 presents the reversible logic gates with its cost those are used to design sequential circuits. Section 5 presents the comparative study about different design of sequential circuits and finally this paper is concluded with section 6.

2   Design Issues of Reversible Sequential Circuit

A sequential circuit consists of a combinational circuit to which memory elements are connected to form a feedback path. It receives binary information from external inputs, combine with the present state of memory elements and determine the binary value at the output terminals. That means a sequential circuit is specified by a time sequence of inputs, outputs and internal states. The external outputs in a sequential circuit are a function of external input and present state of memory element. A reversible sequential circuit is reversible if its transition function is constructed by reversible logic [4]. The transition function acts as a combinational reversible circuit [4]. The functionality of combinational reversible circuit is implemented by suitable reversible gate.

One of the issue that sequential circuit requires a feedback from one of the previous outputs but reversible logic gate does not allow a fan out from one signal [5]. For this 2-bit Toffoli gate is used to make duplicate signal [4]. Optimized design of reversible sequential circuit is another issue.

3   Optimization Parameters

In this paper, we have considered eight optimization parameters forevaluation and comparing among different design of reversible sequential circuits. From the survey of reversible circuits, it is observed that all eight optimization parameters are equally important to synthesis and it plays a pivotal role for the design of optimized reversible circuits.

3.1 Number of Gate (NG): Total number of gates used in circuit. It is proportional to circuit complexity. Minimum possible number of gates makes the circuit efficient.

3.2 Quantum Cost (QC): Total number of quantum gates used in circuit. It is very difficult to count the number of quantum gate of a circuit. So, the quantum cost of all 1x1 and 2x2 reversible gates are considered as unity [7]. Using the quantum constant of this unity we calculate the quantum cost of other circuit.

3.3 Delay (Del): The delay of a circuit is the maximum number of gates in a path from any input line to any output line [6]. In most cases delay has been calculate by the quantum cost.

3.4 Constant Input (CI): It is also known as Ancilla Input. The number of constant value (either 0 or 1) gives as an input to synthesize the logical function. Minimize possible constant input makes the circuit more generalized.

3.5 Garbage Output (GO): Unwanted output in circuit is called garbage output. Its present violate the reversibility of the circuits. Minimum number of garbage output makes the high performing reversible circuit.

3.6 Gate Level (GL): The number of level in the circuits. The level indicates that the output of one gate acts as a input of other gates. Its are required to realize the given logical function [6]. Minimization of gate level reduces the complexity of circuits.

3.7 Hardware : Complexity (HC): Its refer the number of AND, NOT and EX-OR operation present in circuit. It is shown that these three operations are functionally complete. That means using these operation we can implement any logical functionality. Minimization of these operations reduces the circuit complexity and cost. In this paper we consider α as a two input EX-OR operation, β as a two input AND operation and γ as a NOT operation.

3.8 Type of Gate (TG): The number of different type of gates is used in the circuit. Maximization of type of gate is responsible for increase of manufacturing complexity of circuit.

4   Reversible Gate

It is observed that the optimization parameters have not been considered properly in many proposed reversible circuits while designing. In this paper we calculate the quantum cost (QC) and Hardware Complexity (HC) with their reversible representation of the following reversible gates which is not mentioned in the respective paper.

4.1 MG-1 gate [8]: It is a 4x4 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 1. The quantum cost of MG-1 gate is 8. The hardware complexity is $5\alpha+6\beta+4\gamma$.

(a) Block diagram

(b) Reversible Implementation

Fig 1: MG-1 gate and its reversible implementation

4.2 MG-2 gate [8]: It is a 4x4 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 2. The quantum cost of MG-2 gate is 7. The hardware complexity is $3\alpha+4\beta+3\gamma$.
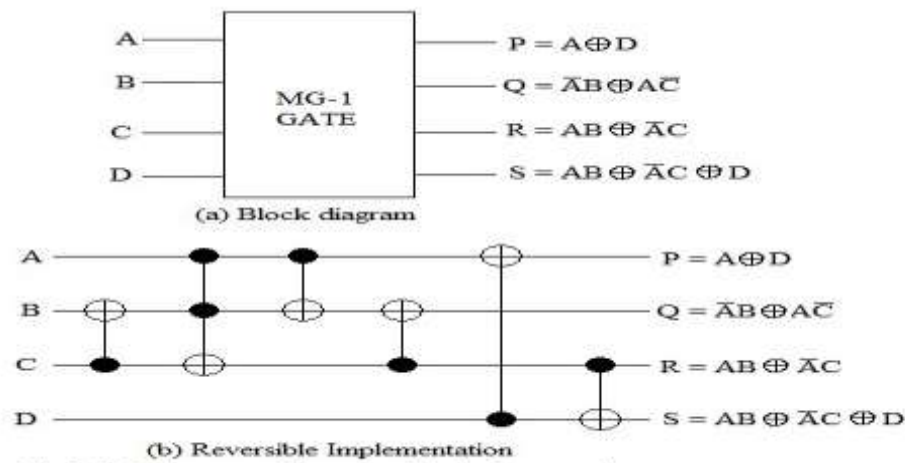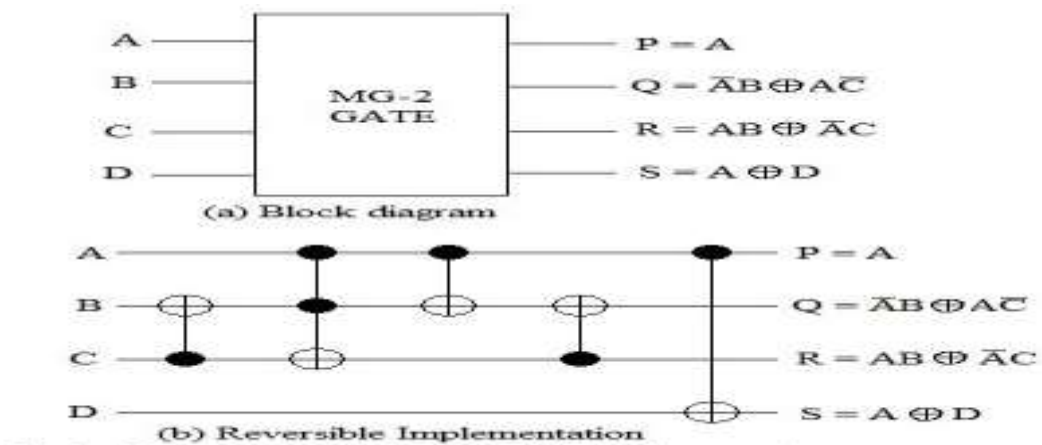

(a) Block diagram

(b) Reversible Implementation

Fig 2: MG-2 gate and its reversible implementation

4.3 SG gate [6]: It is a 4x4 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 3. The quantum cost of SG gate is 9. The hardware complexity is $5\alpha+6\beta+3\gamma$.
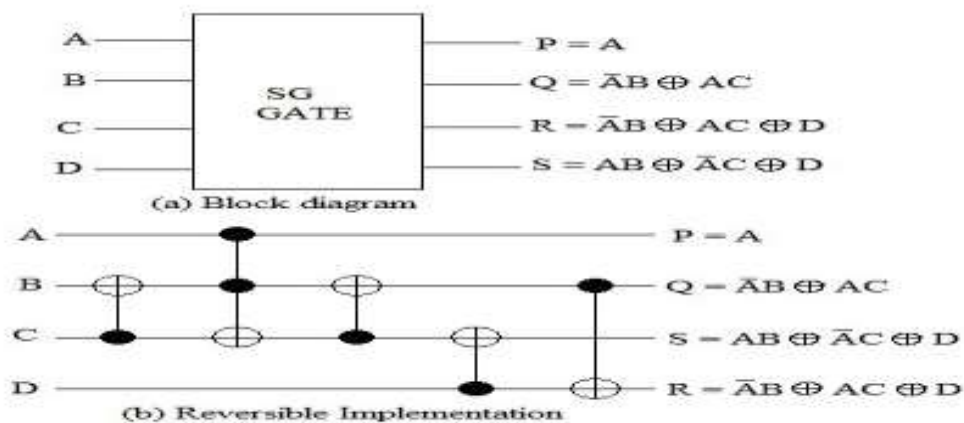

(a) Block diagram

(b) Reversible Implementation

Fig 3: SG gate and its reversible implementation

4.4. NG gate [10]: It is a 3x3 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 4. The quantum cost of NG gate is 11. The hardware complexity is $2\alpha+2\beta+3\gamma$.
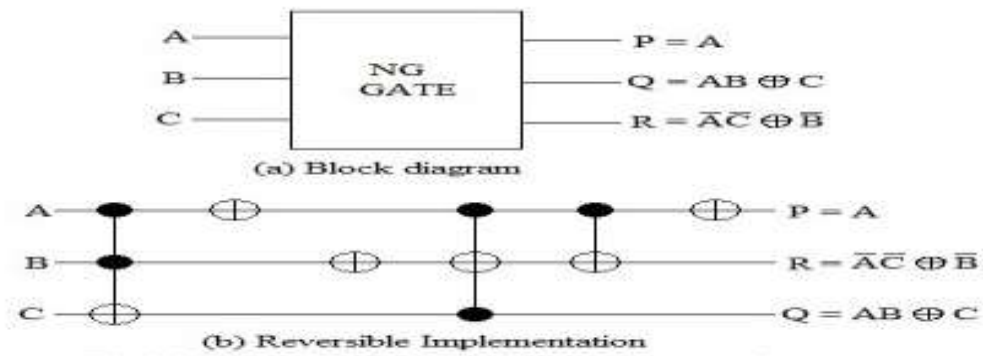
Fig 4: NG gate and its reversible implementation

4.5 BME gate [11]: It is a 4x4 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 5. The quantum cost of BME gate is 15. The hardware complexity is $4\alpha+3\beta+\gamma$.

Fig 5: BME gate and its reversible implementation

4.6 URG gate [5]: It is a 3x3 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 6. The quantum cost of URG gate is 7. The hardware complexity is $4\alpha+2\beta$.

Fig 6: URG gate and its reversible implementation

4.7 VB-1 gate[12]: It is a 4x4 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 7. The quantum cost of VB-1 gate is 11. The hardware complexity is $4\alpha+5\beta+4\gamma$.

Fig 7: VB-1 gate and its reversible implementation

4.8 VB-2 gate[12]: It is a 4x4 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 8. The quantum cost of VB-2 gate is 8. The hardware complexity is $3\alpha+4\beta+4\gamma$.
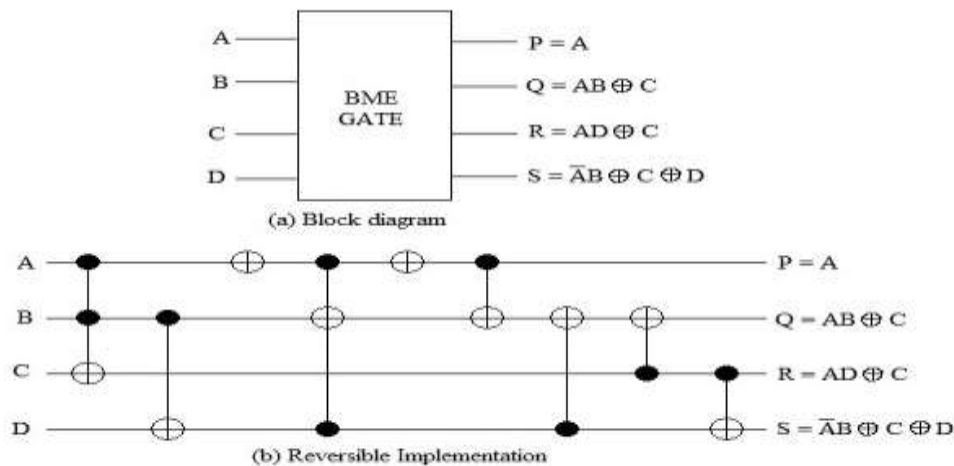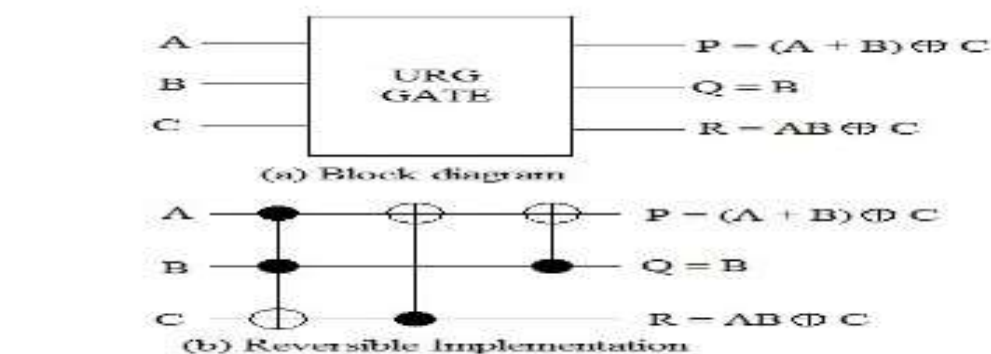

Fig 8: VB-2 gate and its reversible implementation

4.9 RSJ gate [14]: It is a 4x4 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 9. The quantum cost of RSJ gate is 10. The hardware complexity is $2\alpha+2\beta$.

Fig 9: RSJ gate and its reversible implementation

4.10 Mux gate [19]: It is a 3x3 reversible gate. The block diagram with its functionality and reversible implementation is given in Fig. 10. The quantum cost of MUX gate is 5. The hardware complexity is $3\alpha+2\beta+\gamma$.
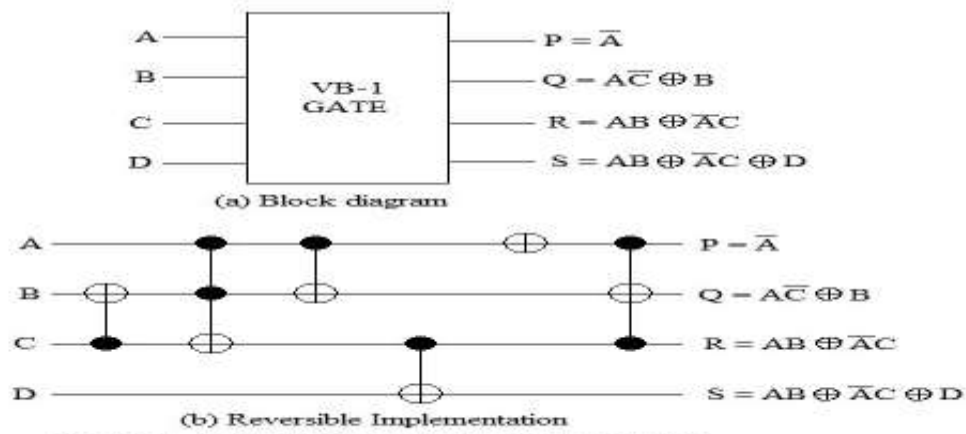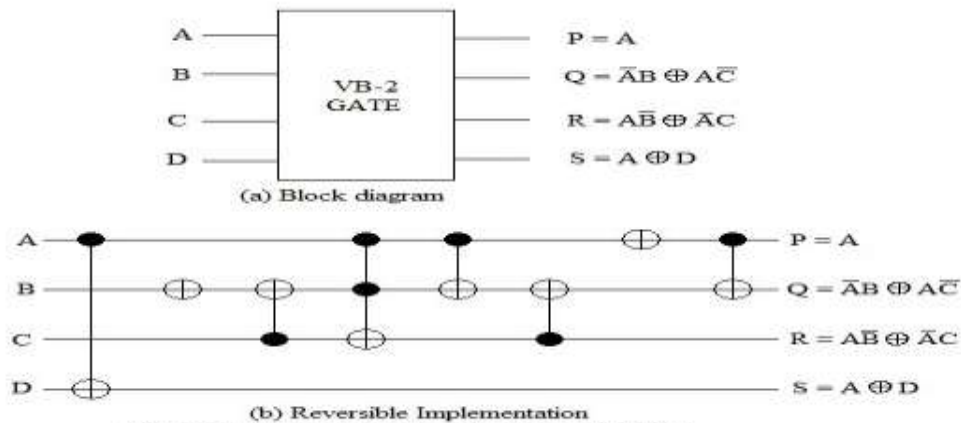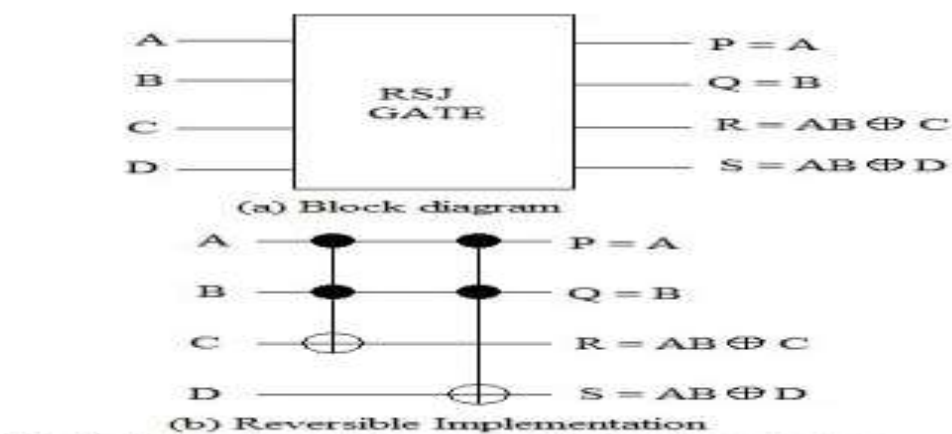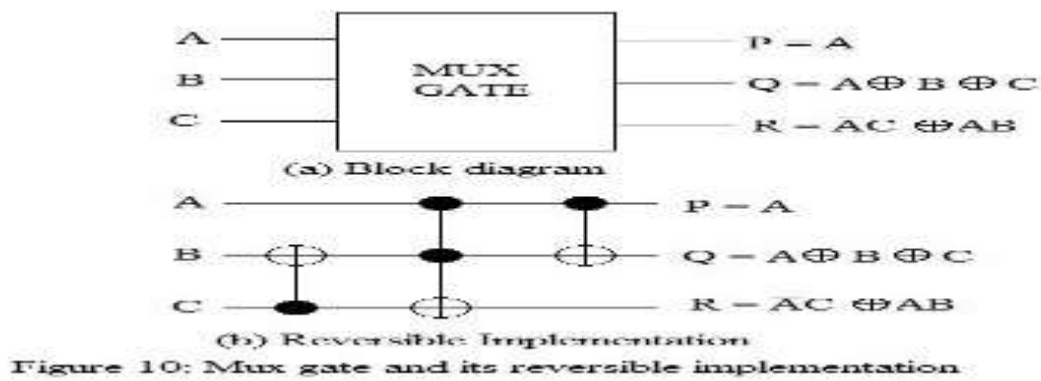
Figure 10: Mux gate and its reversible implementation

5   Reversible Flip Flop Components

A flip flop is a clocked sequential circuit. It is capable of storing binary information and it is affected only with the change of clock pulse. A flip flop has two outputs, one in normal binary form and the other one is its complement. We have considered only reversible flip flops that are synthesized using reversible logic. In the following section, we make a survey on RS-Flip flop, JK- Flip flop, D- Flip flop, T- Flip flop and Master-Slave Flip flop.

5.1 RS- Flip flop: RS-Flip flop is a three input flip flop. The characteristic equation is derived as bellow:

$$Q_{t+1} = \overline{C_p}Q_t + C_pS + Q_t\overline{R} \text{ and } SR = 0$$

The SR=0 specifies that both S, R cannot equal to 1 simultaneously. For this input combination, the intermediate condition occurs. During the survey, we observe that in most cases all the irreversible gates are replaced by different reversible gate to design RS- Flip flop. Table 1 shows the comparison among the existing reversible RS-Flip flop in terms of various optimization parameters.

Table1. Comparison among existing RS-Flip flop

NG	TG	QC	Del	CI	GO	GL	HC
Name of the circuits							
RS-Latch without complemented output using Feynman & Peres gate [13]							
4	2	7	7	1	2	4	$5\alpha+\beta$
RS-Latch without complemented output using Feynman & Toffoli gate [13]							
4	2	8	8	1	3	4	$4\alpha+\beta$
RS-Latch using Peres gate [13]							
2	1	8	8	2	2	2	$4\alpha+2\beta$
RS-Latch using URG gate [5]							
2	1	14	14	2	2	2	$8\alpha+4\beta$
RS-Flip flop using PG gate [9]							
4	1	16	12	4	5	3	$8\alpha+4\beta$
RS- Flip flop using BME & Peres gate [11]							
3	2	23	23	3	4	3	$8\alpha+5\beta+\gamma$
RS-Flip flop using Fredkin & Feynman gate [18]							
6	2	30	23	6	8	3	$10\alpha+16\beta+8\gamma$
RS-Flip flop using NG, Fredkin & Feynman gate [10]							
6	3	38	38	6	8	3	$10\alpha+12\beta+10\gamma$

5.2 D-Flip flop: D- Flip flop is a two input flip flop. The characteristic equation is derived as bellow:

$$Q_{t+1} = \overline{C_p}Q_t + C_pD$$

It has the ability to hold the data into its internal storage. The clock pulse (C_p) is used to transfer the data from input to output. During the survey, we observe that in most cases proposed a new reversible gate and realized by it. Their main objective is to optimize the cost of circuit. Table 2 shows the comparison among the existing reversible D-Flip flop in terms of various optimization parameters.

Table2. Comparison among existing D-Flip flop

NG	TG	QC	Del	CI	GO	GL	HC
Name of the circuits							
D-Latch without complemented output using Fredkin & Feynman gate [4][13]							
2	2	8	8	1	1	2	$3\alpha+4\beta+2\gamma$
D-Flip flop using MG-1 gate [8]							
1	1	8	8	1	1	1	$5\alpha+6\beta+4\gamma$
D Flip flop using Fredkin and Feynman gate [9]							
3	2	9	9	2	2	3	$4\alpha+4\beta+2\gamma$
D-Flip flop using SG & Feynman gate [6]							
2	2	10	10	2	2	2	$5\alpha+6\beta+4\gamma$
D-Flip flop using VB-1 & Feynman gate [12]							
2	2	12	12	2	3	2	$5\alpha+5\beta+4\gamma$
D-Flip flop using BME & Peres gate [11]							
3	2	23	23	3	4	3	$8\alpha+5\beta+\gamma$
D-Flip flop using Fredkin & Feynman gate [18]							
7	2	31	24	7	8	4	$11\alpha+16\beta+8\gamma$
D-Flip flop using NG, Fredkin & Feynman gate [10]							
7	2	47	47	7	8	4	$11\alpha+8\beta+12\gamma$

5.3 JK-Flip flop: JK-Flip flop is a three input flip flop. It is a refinement of RS-Flop flop that remove the intermediate state. The characteristic equation is derived as bellow:

$$Q_{t+1} = \overline{C_p}Q_t + Q_t\,\overline{K} + C_p\overline{Q_t}J$$

When both input (J and K) are 1 and the clock pulse remain enable then the output will be complement or toggle until the clock pulse goes back to disable. During the survey, we observe that in most cases proposed a new reversible gate and realized by it. Their main objective is to optimize the cost of circuit. Table 3 shows the comparison among the existing reversible JK-Flip flop in terms of various optimization parameters.

Table3. Comparison among existing JK-Flip flop

NG	TG	QC	Del	CI	GO	GL	HC
Name of the circuits							
JK-Latch using Fredkin & Feynman gate [13]							
5	3	16	16	2	3	5	$6\alpha+8\beta+5\gamma$
JK-Latch without complemented output using Toffoli & Feynman gate [4]							
4	3	32	32	1	2	4	$8\alpha+7\beta$
JK-Flip flop using MG-1 & MG-2 gate [8]							

2	2	15	15	2	2	2	8α+10β+7γ
JK-Flip flop using Fredkin & Feynman gate [9]							
4	2	16	16	2	2	4	6α+8β+4γ
JK-Flip flop using SG, Fredkin & Feynman gate [6]							
3	3	17	17	2	3	3	7α+10β+6γ
JK-Flip flop without complemented output using VB-1 & VB-2 gate [12]							
2	2	19	19	2	3	2	7α+9β+8γ
JK-Flip flop using Fredkin & Feynman gate [10]							
10	3	54	54	10	12	5	16α+20β+14γ

5.4 T-Flip flop: T-Flip flop is a two input flip flop. The characteristic equation is derived as bellow:

$$Q_{t+1} = \overline{C_p}Q_t + Q_t\,\overline{T} + C_p\overline{Q_t}T$$

It has the ability to toggle its output. During the survey, we observe that in most cases proposed a new reversible gate and realized by it. Their main objective is to optimize the cost of circuit. Table 4 shows the comparison among the existing reversible JK-Flip flop in terms of various optimization parameters.

Table4. Comparison among existing T-Flip flop

Name of the circuits							
NG	TG	QC	Del	CI	GO	GL	HC
T-Latch without complemented output using Toffoli & Feynman gate [4]							
2	2	6	6	1	1	2	2α+β
Clocked T-Flip flop using Peres gate & Feynman gate [7][36]							
2	2	5	5	1	1	2	3α+β
T-Flip flop using Peres gate & Feynman gate [9][13][36]							
3	2	6	6	2	2	3	4α+β
Clocked T-Flip flop using Mux & Double Feynman gate [19][36]							
2	2	7	6	1	2	2	5α+2β+γ
T-Flip flop without complemented output using Fredkin & Feynman [5][36]							
3	2	9	9	1	2	3	4α+4β+2γ
T-Flip flop using VB-1 & Feynman gate [12]							
3	2	13	13	2	2	3	6α+5β+4γ
Clocked T-Flip flop using Fredkin & Feynman gate [16]							
5	2	17	17	2	3	5	7α+8β+4γ
Clocked T-Flip flop using SG & Feynman gate [14]							
3	2	19	19	2	3	3	11α+8β+6γ
T-Flip flop using NG, Fredkin & Feynman gate [10]							
10	3	54	54	10	12	5	16α+20β+14γ

5.5 Master-Slave Flip flop: A Master-Slave flip flop is the combination of two separate flip flops. One acts as a master and other as a slave. During the survey, we observe that in most cases it is realized by proposed reversible flip flop. Their main objective is to optimize the cost of circuit. Table 5 shows the comparison among the existing reversible Master-Slave flip flop in terms of various optimization parameters.

Table5. Comparison among existing Master-Slave Flip flop

NG	TG	QC	Del	CI	GO	GL	HC
Name of the circuits							
Master Slave RS-Flip flop without complemented output using Fredkin, Toffoli & Feynman gate [13]							
6	3	16	16	2	3	6	$7\alpha+5\beta+2\gamma$
Master Slave D-Flip flop without complemented output using Fredkin & Feynman gate [13]							
4	2	16	16	2	2	4	$6\alpha+8\beta+2\gamma$
Master Slave D-Flip flop using MG-1 gate [8]							
2	1	16	16	2	2	2	$10\alpha+12\beta+8\gamma$
Master Slave D-Flip flop without complemented output [4]							
5	3	16	16	2	2	5	$6\alpha+8\beta+5\gamma$
Master Slave D-Flip flop using VB-1 & Feynman gate [12]							
3	2	23	23	3	2	3	$9\alpha+10\beta+8\gamma$
Master Slave JK-Flip flop using MG-1 & MG-2 gate [8]							
3	2	23	23	3	3	3	$13\alpha+16\beta+11\gamma$
Master Slave JK-Flip flop without complemented output using Fredkin & Feynman gate [13]							
6	3	23	23	2	3	6	$8\alpha+12\beta+7\gamma$
Master Slave JK-Flip flop without complemented output using VB-1 & VB-2 [12]							
3	2	30	30	3	3	3	$11\alpha+14\beta+12\gamma$
Master Slave JK-Flip flop without complemented output [4]							
7	5	40	40	2	3	6	$11\alpha+11\beta+3\gamma$
Master Slave JK-Flip flop using NG, Fredkin, Feynman gate [10]							
18	3	110	110	18	21	8	$28\alpha+24\beta+28\gamma$
Master Slave T-Flip flop without complemented output using Peres, MPG, Feynman gate [7]							
4	3	10	10	2	3	4	$6\alpha+2\beta+\gamma$
Master Slave T-Flip flop without complemented output using Peres , Feynman & Fredkin gate [13]							
4	3	13	13	2	0	4	$6\alpha+5\beta+2\gamma$
Master Slave T-Flip flop without complemented output [4]							
5	4	14	14	2	2	5	$5\alpha+5\beta+3\gamma$
Master Slave T-Flip flop using VB-1 & Feynman gate [12]							
4	2	24	24	3	1	4	$10\alpha+10\beta+8\gamma$

6. Reversible Flip Flop Components

6.1 Reversible Counter: Counter is sequential circuit that goes through a prescribed sequence of states upon the application of input pulse. A n-bit reversible counter [37] consists of n reversible flip flops. Counter is categorized into two types: Synchronous and Asynchronous. In synchronous counter, the clock pulse is applied as input of flip flops. In asynchronous counter the output of one flip flop is

applied to the clock pulse of other flip flop respectively except the first flip flop. The clock pulse is applied directly to the clock pulse of the first flip flop. During the survey, we observed that it is realized by proposed flip flop and optimize the cost of circuit. Here we calculate the values of optimization parameters which is not mentioned in the respective paper. Table 6 shows the comparison among the existing reversible counter in terms of various optimization parameters.

Table6. Comparison among existing Reversible Counter

NG	TG	QC	Del	CI	GO	GL	HC
Name of the circuits							
4-bit Synchronous counter [22]							
12	3	32	32	8	5	12	$17\alpha+7\beta$
4-bit Synchronous counter [7]							
12	3	36	36	8	6	12	$18\alpha+12\beta+4\gamma$
4-bit Synchronous up-down counter [19]							
10	4	41	37	7	9	10	$29\alpha+10\beta+4\gamma$
4-bit Synchronous down counter [14]							
7	3	100	100	13	16	7	$50\alpha+37\beta+24\gamma$
4-bit Synchronous up-down counter [14]							
10	3	127	117	18	20	10	$56\alpha+50\beta+30\gamma$
4-bit asynchronous counter [22]							
8	3	23	23	4	1	8	$9\alpha+4\beta$
4-bit asynchronous counter [7]							
8	3	23	23	7	5	8	$15\alpha+4\beta$
4-bit asynchronous counter [20]							
12	3	36	36	8	6	12	$18\alpha+12\beta+4\gamma$
4-bit asynchronous counter [21]							
23	2	71	71	15	12	12	$31\alpha+4\beta+2\gamma$
4-bit asynchronous up-down counter [16][36]							
7	2	71	71	8	16	7	$31\alpha+32\beta+16\gamma$
4-bit asynchronous up-down counter [17][36]							
8	2	72	72	8	13	8	$32\alpha+32\beta+16\gamma$
4-bit asynchronous up-down counter [15][36]							
7	2	79	79	8	16	7	$47\alpha+32\beta+24\gamma$
4-bit asynchronous up counter [18]							
28	2	124	92	28	32	16	$44\alpha+64\beta+32\gamma$

6.2 Reversible Register: A register is suitable for holding binary information. An n-bit register have a group of n flip flops. It is referred as parallel load that means all the bits of the register are loaded simultaneously with a single clock pulse. Shift register is capable of shifting its binary information either to the right or left. All modes of operation of a universal shift register such as SISO (serial-in-serial output), SIPO (serial-in-parallel output), PISO (parallel-in-serial output) and PIPO (parallel-in-parallel output) can also be performed upon the occurrence of clock. Table 7 shows the comparison among the existing reversible universal shift register in terms of various optimization parameters.

Table 7. Comparison among exiting Reversible Universal Shift Register

NG	TG	QC	Del	CI	GO	GL	HC
Name of the circuits							
Universal Shift Register [30]							
26	-	94	-	14	19	-	-
Universal Shift Register using FF-I& Mux-II [27]							
34	-	98	-	18	21	-	-
Universal Shift Register using FF-I& Mux-I [27]							
41	-	108	-	28	33	-	-
Universal Shift Register [26]							
-	-	110	-	-	36	-	-
Universal Shift Register using FF-III& Mux-I [27]							
40	-	110	-	30	37	-	-
Universal Shift Register using FF-III & Mux-II [27]							
33	-	110	-	20	25	-	-
Universal Shift Register [25]							
-	-	114	-	-	40	-	-
Universal Shift Register [28]							
-	-	114	114	-	40	-	-
Universal Shift Register [24]							
-	-	120	-	-	36	-	-
Universal Shift Register using FF-II & Mux-II [27]							
41	-	120	-	24	29	-	-
Universal Shift Register using FF-II & Mux-I [27]							
48	-	130	-	34	41	-	-
Universal Shift Register [23]							
-	-	144	-	-	40	-	-
Universal Shift Register [29]							
48	-	144	-	24	31	-	-

6.3 Reversible RAM: The 2^n x m memory consists 2^n words with n bit address line and m bit in each words. It has total $(2^n.m)$ numbers of binary cells. Each binary cell contains one flip flop, three 3input AND gate and two NOT gate. The n bit address goes through n x 2^n decoder. During the survey, we observe that the construction of reversible RAM is the realization of all the irreversible components by reversible components. Their main focus is to reduce the power consumption/dissipation, quantum cost, number of garbage output and gate count. Table 8 shows the comparison among the existing reversible RAM.

Table 8. Comparison among exiting Reversible RAM

NG	QC	GO	PC/PD*
Name of the circuits			
2^n x m PRAM [31]			
696	120	1243	112 mV
2^n x m Reversible RAM [32]			
$2^n (8m+2)-1$	$58m+4.2^n -7$	$2^n (7m+3)+n$	-
2 x 4 RAM [33]			
30	-	9	29 mW
2^n x m Reversible RAM [34]			
$2^n(6m+2)+m-1$	$2^n (19m+9)-7$	$m.(4.2^n -1)+n$	-
2^n x m PPRRAM [35]			
$2^{n-1}(9m+5)+m-1$	-	$2^n(4m+4)+m.n$	-

*PC/PD = Power Consumption / Power Dissipation.

7. Conclusion

Designing optimized sequential reversible circuit is always a challenging task. In this paper we compute the respective optimization parameters which are not present in the existing available literature. At the same time a comparative table has been shown for better understanding of the state of art work. In this way the paper helps researchers to understand the current state of work and helps them to focus on the more optimized design and efficient reversible circuit.

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