Design of Power Efficient Phase Frequency Detector and Voltage Controlled Oscillator for PLL Applications in 45 nm CMOS Technology

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ABSTRACT:*A novel phase frequency detector is designed which is made up of 16 transistors whereas conventional is of 48 transistors. This paper also presented the design of charge pump circuit and current starved VCO (CSVCO). These are the critical blocks that are widely used for applications like clock and data recovery circuit, PLL, frequency synthesizer. The proposed PFD eliminates the reset circuit using pass transistor logic and operates effectively at higher frequencies. The circuits are designed using Cadence Virtuoso v6.1 in 45nm CMOS technology having supply voltage 1V. It was found that the power consumption of PFD is 138.2 nW which is significantly lesser than other designs. CSVCO also analysed at operating frequency of 10 MHz to give output oscillation frequency of 1.119 GHz with power dissipation of 18.91 µW. Corner analysis done for both the PFD and CSVCO for various process variations. Monte Carlo analysis also done for the proposed PFD and presented CSVCO to test the circuit reliableness.*

Keywords: PLL, Phase frequency detector, Charge pump, CSVCO, low power.

1.INTRODUCTION

Phase locked loop (PLL) is a nonlinear feedback system which is a critical electronic component and extensively used in applications like frequency synthesizers, clock and data recovery, modulation and demodulation of FM wave, jitter attenuator and networking etc. The block diagram of PLL which comprises of VCO, charge pump, phase frequency detector (PFD) etc. PFD and VCO are one of the critical blocks of PLL and works as comparator. PFD increases the speed of PLL by increasing its acquisition range. PLL performance is also influenced by another key block known as Charge pump. It generates the single control output signal based on the logic state of comparator (PFD) for proper functioning of VCO.

In this paper [1], asynchronous race free design of PFD using D flip flop where D=1 is given but its power consumption is very high. In another work, a precharged type ncPFD is presented with delay stages added to provide zero dead zone [2] but its maximum operating frequency is less. An open loop, highly accurate PFD with wide frequency range is presented in [3] but power is in milliwatt range. In this paper, a modified precharged type PFD by inserting delay cells [4] is given but area is increased. In one of the previous arts a VCO with full switching differential delay cell was shown but tuning range was restricted [5]. In other paper a CMOS VCO using diode connected PMOS transistors for tuning the current was presented but its drawbacks are narrower frequency range with excessive power [6]. In other work, a three stage VCO using differential pair NMOS and PMOS load transistor composed delay cell is presented but consumes large power [7]. When VCO is implemented using CMOS current- mode logic stages, frequency range is widened by using ring oscillator structure, but power consumption is very high [8]. To obtain a low power phase frequency detector and wide frequency range ring based VCO with low power consumption is one of the great challenges in the previous works. In this paper, a proposed phase frequency detector is given with 16 transistors which

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has lesser power consumption, larger operating frequency is given and current starved VCO is presented which has lower power consumption and high oscillation frequency. This paper is formed as follows: Section 2 explains the proposed phase frequency detector and charge pump. Section 3 explains the Current starved VCO with the circuit diagram. Section 4 shows the simulation analysis and result discussion of the proposed PFD ,presented charge pump and VCO. Section 5 is the conclusion.

2.Circuit Description

2.1 Proposed Phase Frequency Detector

PFD is one of the critical blocks of PLL and works as comparator. PFD increases the speed of PLL by increasing its acquisition range. The most popular PFD made up of two D flip flops and a logic gate [9] however its drawback is off higher power consumption of traditional PFD, some modification has been done to remove the reset path. The proposed phase frequency detector solves the problem higher power consumption and lower operating frequency. Figure1 shows the novel phase frequency detector. Here it contains the 6 PMOS transistors and 10 NMOS transistors.

The operation of proposed PFD is that initially assume both inputs (feedbackClk and refClk) of PFD are at low voltage level. Then, MP_1 and MP_2 transistor turns ON results in output node A to high state. This node A is connected to MN_3 and MN_5 through pass transistor logic and it causes both node X and Y to a low logic level. For the rising edge of the refClk input, node X goes to high logic level through MN_3 transistor and leads to the UP rises and similarly for rising edge of feedbackClk input node Y rises to high logic level through MN_5 transistor causing down signal rises to high voltage level. In a case, where both node X and Y go to high state then they automatically go to low state through MN_4 and MN_6 transistor. Thus, here reset circuit is eliminated with the help of pass transistors. Here, cascading of inverter stages is used just before both output signal UP and DOWN to provide the full swing output and remove the glitches produced. This circuit has also lesser area since only 16 transistors are required. The outputs UP and DOWN can be applied directly to the charge pump circuit.

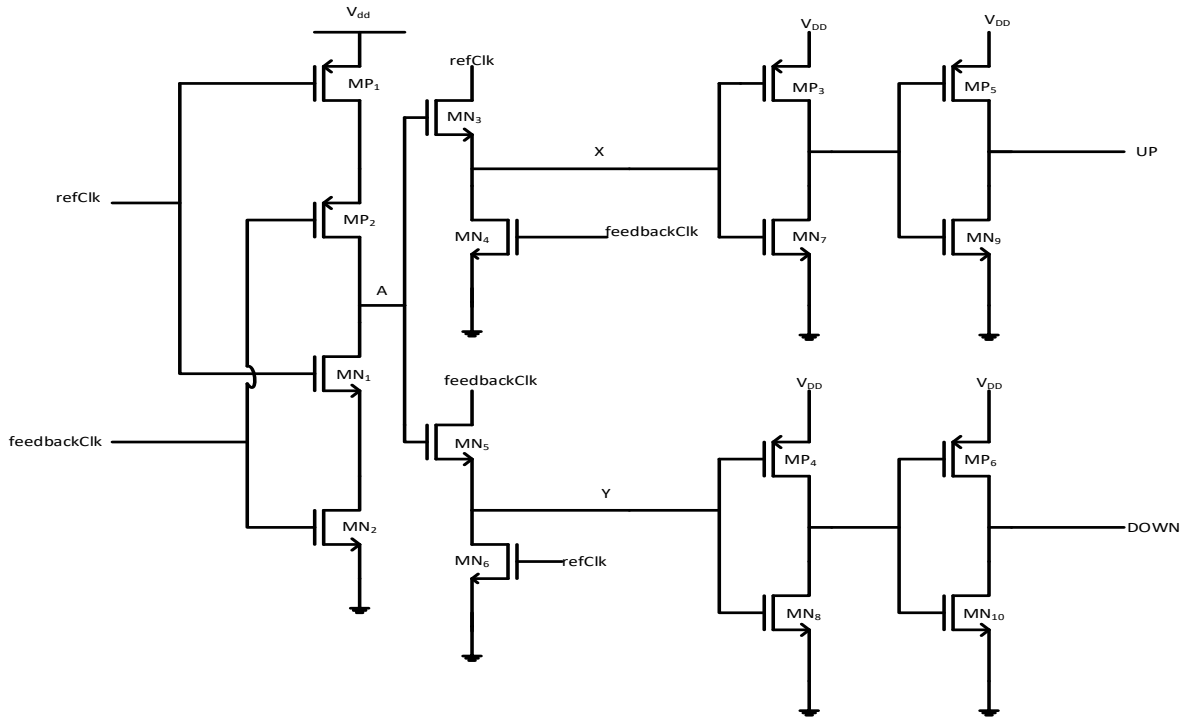

Figure 1. Proposed Phase frequency detector (PFD)

2.2 Charge pump and loop filter

The charge pump is a circuit whose operation is to convert the PFD logic state into an analog signal to control the frequency of the VCO. It is generally connected with the loop filter and placed between the VCO and PFD block. There are various types of charge pumps like Dickson charge pump, current steering charge pump, single-ended and differential charge pump. Figure 2 shows the circuit diagram of charge pump with loop filter. The two outputs of PFD i.e., UP and DOWN are given as an input to the charge pump, and it produces a single output which is fed to the loop filter.

Here its operation is summarized as when UP signal is high and DOWN signal is low then the charging condition is obtained i.e., current across charge pump intrude the loop filter. When UP signal is low and DOWN signal is high then discharging occurs and charge pump current flows out of loop filter. When both the input signals UP and DOWN are at low or high the output of charge pump is constant.

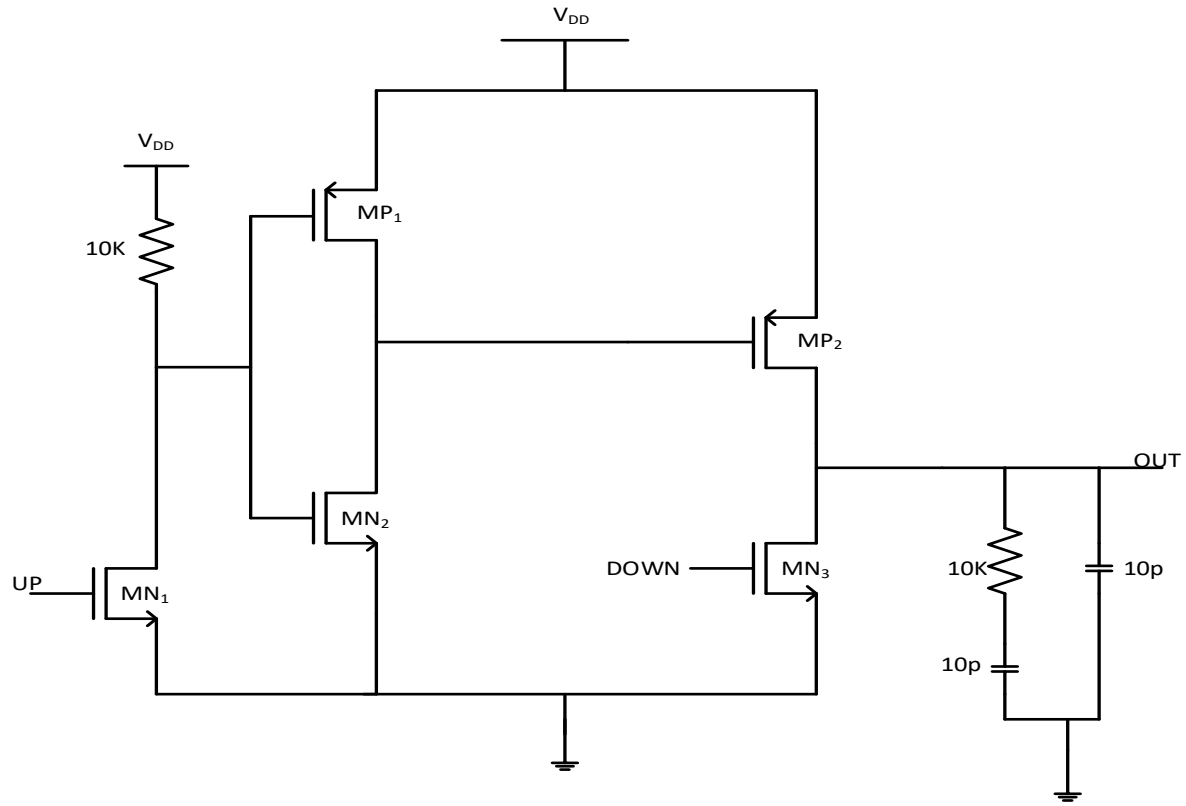

Figure 2. Combined circuit of Charge pump with low pass filter [10]

Loop filter is a critical component which is basically used to remove the noise and increase stability. Loop filter are off various types like LC filter, active and passive low pass filter, RC low pass filter etc. The basic passive low pass filter is used as a loop filter [11] shown in figure3.

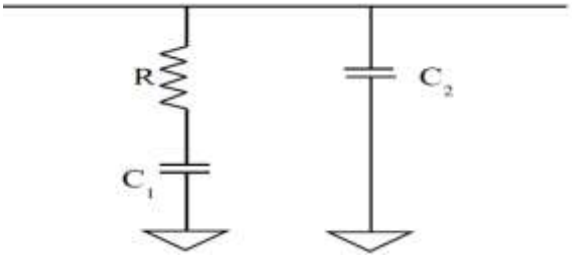

Figure 3. Basic passive low pass filter as Loop filter [11]

The main purpose of a loop filter to transform the output current of charge pump into voltage signal. This is necessary for maintaining the fixed control voltage which is given as an input to the VCO. Here, for efficient output, C_2 value should be one-tenth of C_1 value.

Here, we are using R=10KΩ, C_1=10pF and C_2=1pF. The frequency can be calculated as:

$$f = \frac{1}{2\pi\sqrt{RC_1C_2}} \quad (1)$$

3. Current Starved VCO

The circuit diagram of current starved based VCO [11] is shown in the figure4. It behaves as a ring oscillator. The middle transistors (MP_4 and MN_5) form an inverter while the upper and lower current sources MP_3 and MN_6 drop the current available to the inverter i.e., the inverter is starved for current.

The drain currents of MP_1 and MN_2 are same and are set by input control voltage V_{ctrl} .The currents are mirrored to each inverter stage. The current starved VCO has advantage of wide frequency range and lesser power so it is widely used.

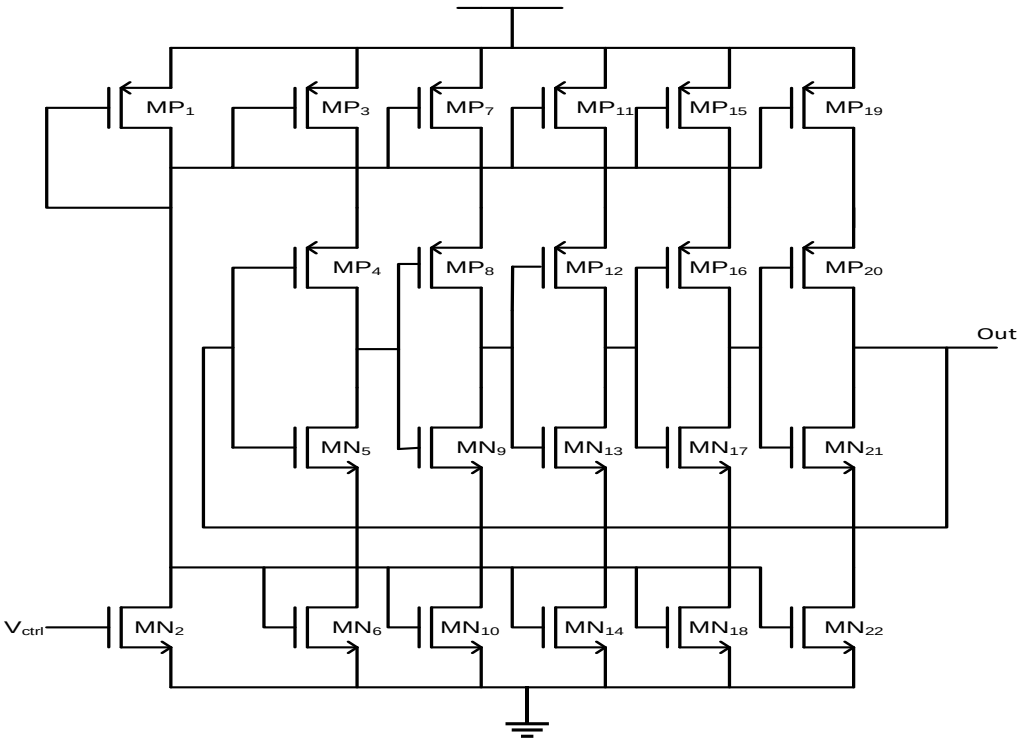

Figure4. Current starved VCO

The oscillation frequency of VCO is the inverse of two times of product of no of inverter stages and propagation delay and given as:

$$f_{OSC} = 1/2N\tau \quad (2)$$

Where N= stages number and τ= propagation delay.

τ can be calculated by considering capacitance on drain side of MP_4 and MN_5 of inverter given as:

$$C_{tot} = 5/2\ C_{ox}\ (W_p\ L_p + W_n\ L_n) \quad (3)$$

Now, the oscillation frequency can be evaluated as:

$$f_{OSC} = 1/N\ (\tau_1 + \tau_2) \quad (4)$$

where τ_1 and τ_2 are the charging and discharging time and calculated with the help of C_{tot}.

In the primary current starved structure, as control voltage changes, the current is mirrored to MP_1 by using the current mirror technique. From the transistor MP_1, the current will be mirrored to all the pull-up PMOS transistors. Its drawback is power consumption is high, so another circuit required to overcome this limitation. Using stacked sleep technique, the power is significantly reduced.

4.Results and Discussion

The circuits are designed and implemented using Cadence Virtuoso V6.1.7. It is basically a circuit simulator tool which provides capabilities of designing and testing of circuit. Here, technology used is gpdk045nm.

4.1 Transient Analysis of proposed PFD

The proposed phase frequency detector shown in figure transient analysis is done using Cadence ADEL tool and output of UP and DOWN signal for all cases shown in figure 5 , 6 ,7.

Case1: Here reference clock and feedback clock both in phase , then both the UP and DOWN signal rises for a very small amount of time on every rising edge as shown in figure 5.

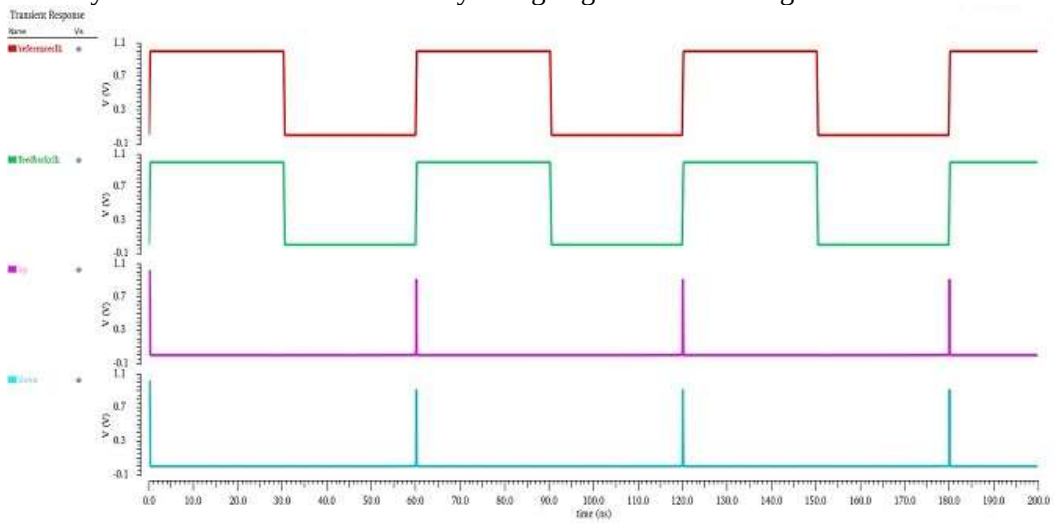

Figure5. Output waveform when both inputs are in phase

Case2: Here rising edge of reference clock leads feedback clock , for that amount of time the UP signal rises as shown in figure 6. Here , the spikes are eliminated for down signal.

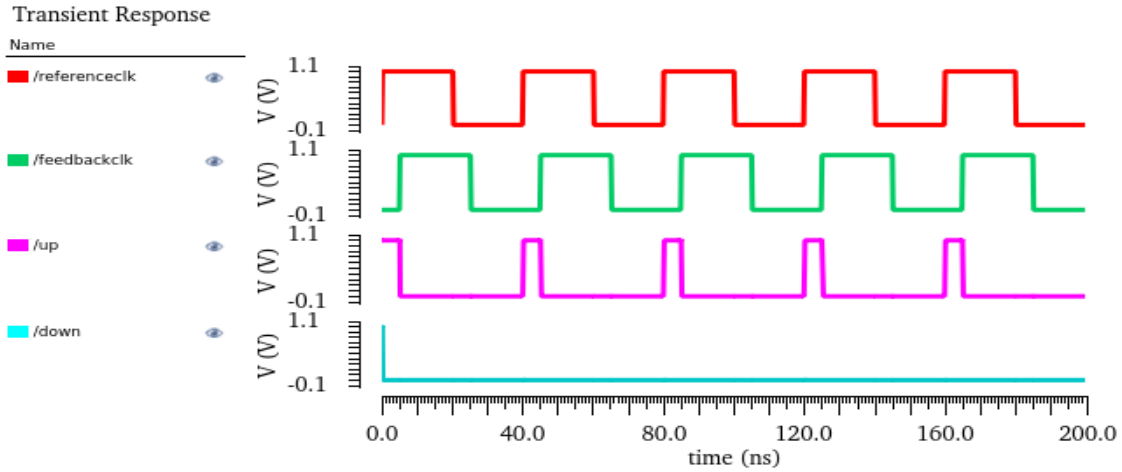

Figure6. Output waveform when reference clock leads feedback clock

Case3: Here, feedback clock rising edge leads reference clock , for that amount of time the DOWN signal rises as shown in figure 7. Here , the spikes are eliminated for UP signal.

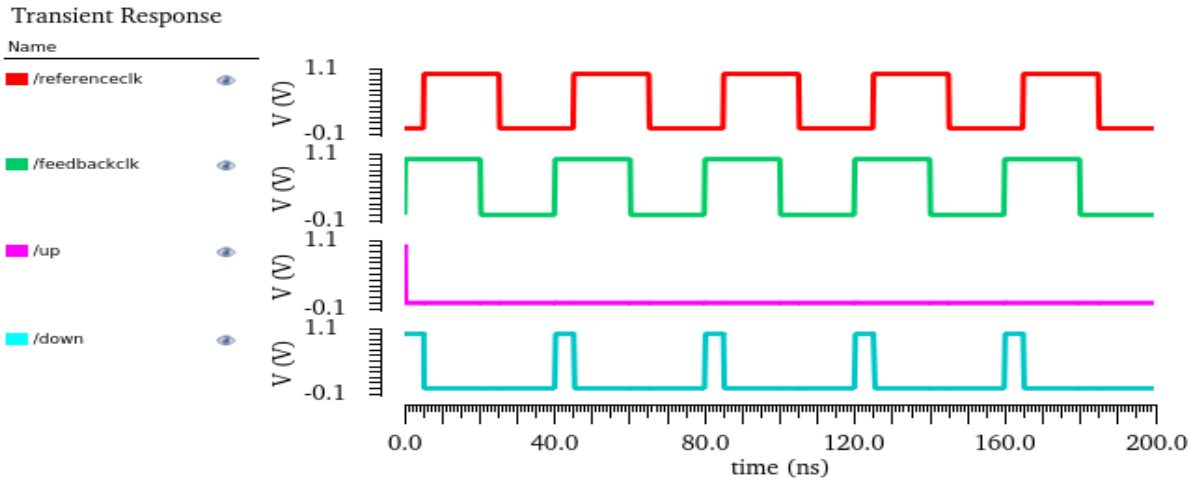

Figure7. Output waveform when feedback clock leads reference clock

4.2Corner analysis

Table 1. Process Corner Analysis of proposed circuit

Parameters	NN	FF	FS	SF	SS
Dynamic power (nW)	132	131.1	108.2	184.1	109.9
Static Power (pW)	28.42	164.5	44.32	30.11	15.34
Total power (nW)	132	131.2	108.2	184.2	109.9
Delay (ps)	690.9	199	281.3	2980	4326
PDP(10^{-18} J)	91.22	26.11	30.44	548.9	475.4

For the fabrication of an IC, various processes like oxidation, lithography, diffusion etc. are done so we tend to not get same result as we want. Corner analysis is done in order to find that how the circuit behaves with process corner variations. The corner analysis done for the proposed PFD are given in table1.

4.3 Monte Carlo Analysis

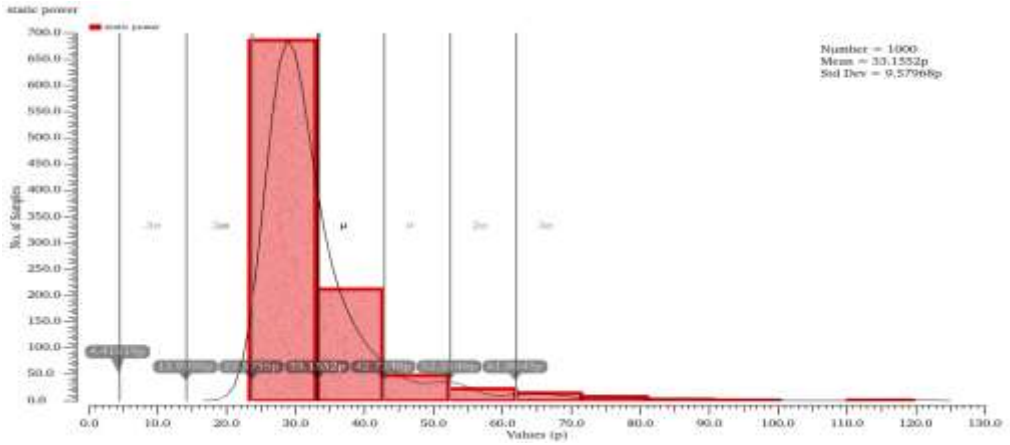

Figure8. Monte Carlo Analysis for static power in proposed circuit

To check the reliability of the circuit, Monte carlo analysis is performed to simulate all the corner regions. Monte Carlo analysis performed for static, dynamic, and total power for 1000 samples. The mean and standard deviation is summarized in table 2.

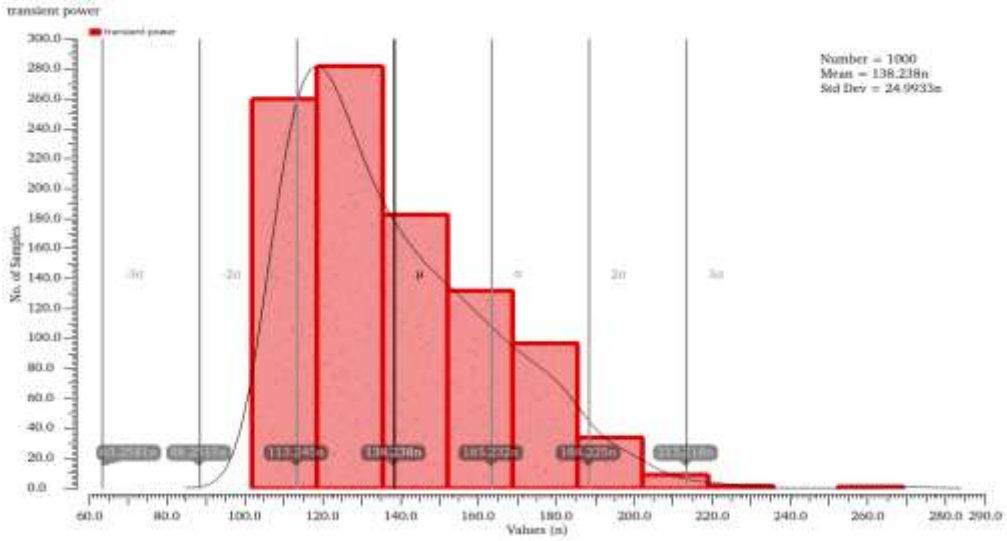

Figure9. Monte Carlo Analysis for transient power in proposed circuit

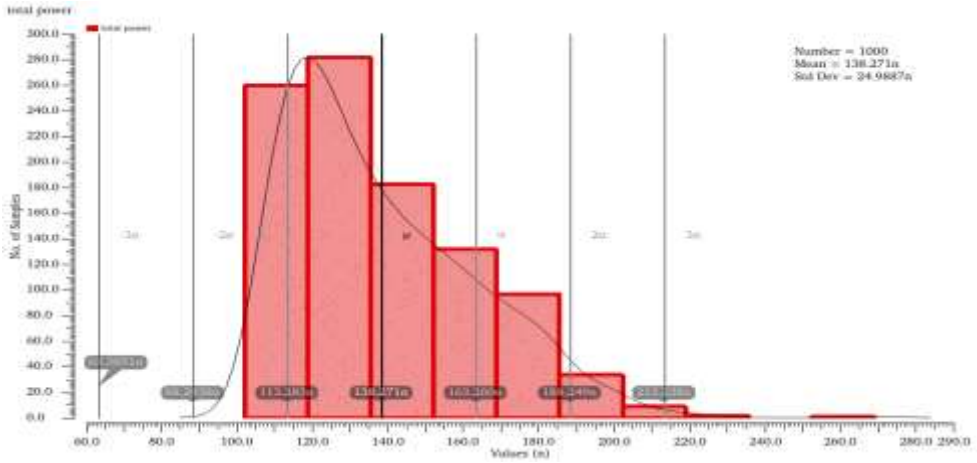

Figure10: Monte Carlo Analysis for total power in proposed circuit

Table2. Summary of Monte carlo analysis for proposed PFD

Parameters	Mean	Standard Deviation
Static power(pW)	33.16	9.58
Dynamic power(nW)	138.2	24.99
Total power(nW)	138.3	24.99

4.4 Transient analysis of Charge pump

The charge pump with loop filter is in figure 2 is simulated with the help of cadence tool and waveform is shown in figure 11. As shown in figure, when up signal is high and down signal is low the charging condition occurs and vice versa is true for the condition of discharging. When both

signals are low or high then out is constant i.e., neither charge nor discharge. The power consumed by this circuit is 79.069µW for the supply voltage of 1V.

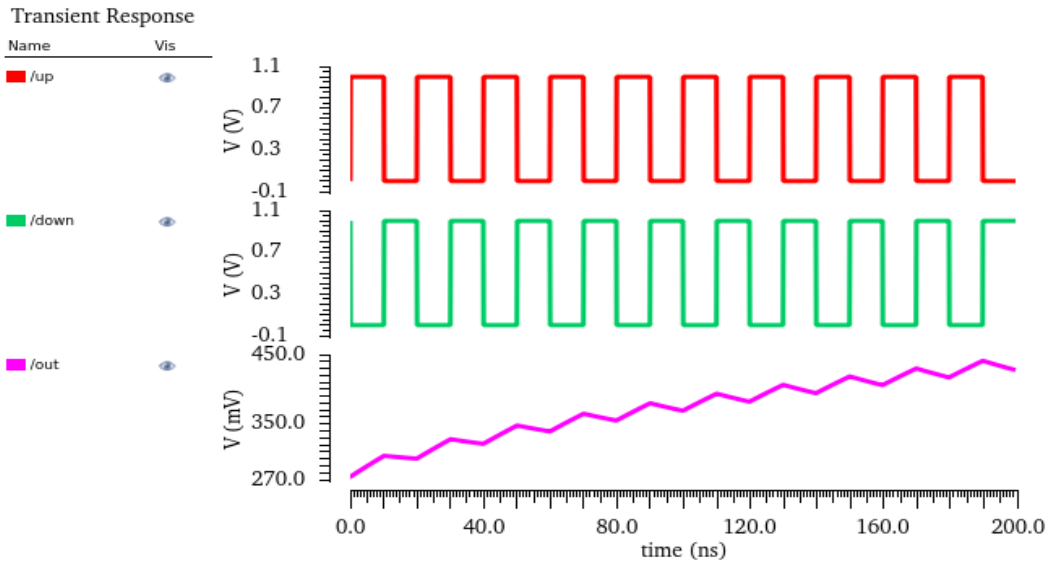

Figure11. Simulation results of charge pump

4.5 Layout of the proposed PFD

The proposed phase frequency detector layout is designed in 45 nm technology with supply voltage of 1V and layout area of the circuit shown in figure 12 is 33.744µm^2.

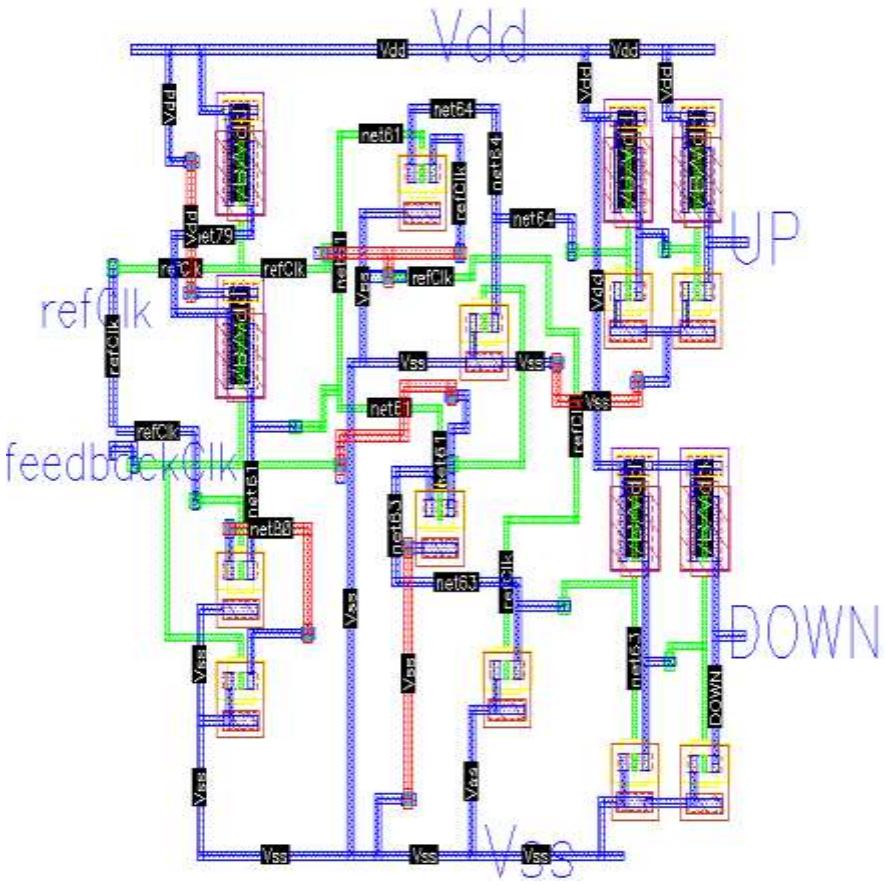

Figure12. Layout of the proposed PFD

4.6 Performance Comparison of proposed PFD with previous works

The work that is proposed is compared with the other designs is shown in table 3. Here, the modified PFD simulation also done, and its parameters are calculated and compared. From the other designs presented here this circuit consumes lesser power , delay and PDP are also very less however operating frequency is lesser than [15].

Table 3. Performance Comparison of proposed PFD with other design

Parameters	Modified PFD	ptPFD[14]	Dynamic TGCMOS[14]	[15]	This work
Supply Voltage	1	2	2	1.8	1
No. of transistors	16	20	24	4	16
Power (µW)	.692	113	706	8	.138
Delay (ns)	40.03	2.49	0.0021	NA	.690
PDP (10^{-15} J)	27.68	281.3	1.48	NA	.0912
Max frequency (GHz)	2.2	NA	NA	5	3.4

4.7 Simulation Oscillations of CSVCO under transient analysis Simulation Oscillations of CSVCO under transient analysis

The transient analysis of current starved sleep VCO is done using Cadence ADEL tool and output waveform is shown in figure 13. Here, control voltage Vctrl set to 1V to give output frequency of 1.12 GHz. Here, when power is calculated using ADEL tool its total power is 18.91 µW.

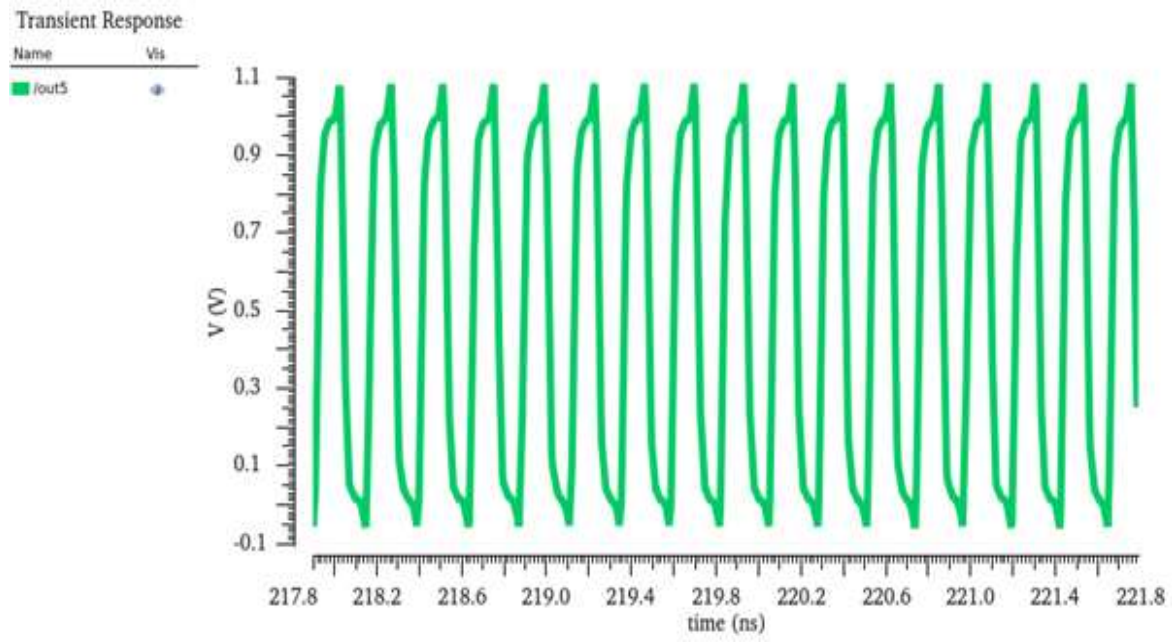

Figure13.Transient analysis of current starved VCO for Vctrl=1V

4.8 Variation of frequency and total power with control voltage (Vctrl) in Current Starved VCO

Table 4 shows the variation of frequency and total power with control voltage (Vctrl) in CSVCO. The applied input control voltage is varied from 0.8 to 1.2V, in steps of 0.1 V, oscillation frequency is calculated in each case for operating frequency of 10 MHz. In each case, total power is also calculated.

Table 4. Variation of frequency and total power with control voltage (V_{ctrl}) in CSVCO.

V_{ctrl} (Control Voltage)	Oscillation frequency (in GHz)	Total power (in µW)
0.8V	.591	8.44
0.9V	.881	13.86
1.0V	1.119	18.91
1.1V	1.305	23.11
1.2V	1.461	26.57

4.9 Frequency vs Voltage variation in CSVCO

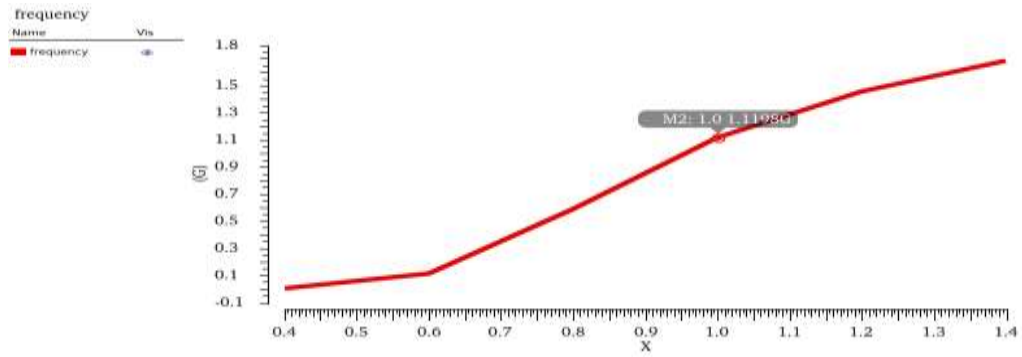

Figure14. Frequency vs V_{ctrl} in proposed VCO

Figure14 gives the plot of frequency changes with respect to control voltage using parametric analysis in ADEL tool. Here as the circuit is given higher control voltage, the frequency is also increased.

4.10 Variation of frequency with respect to temperature in CSVCO

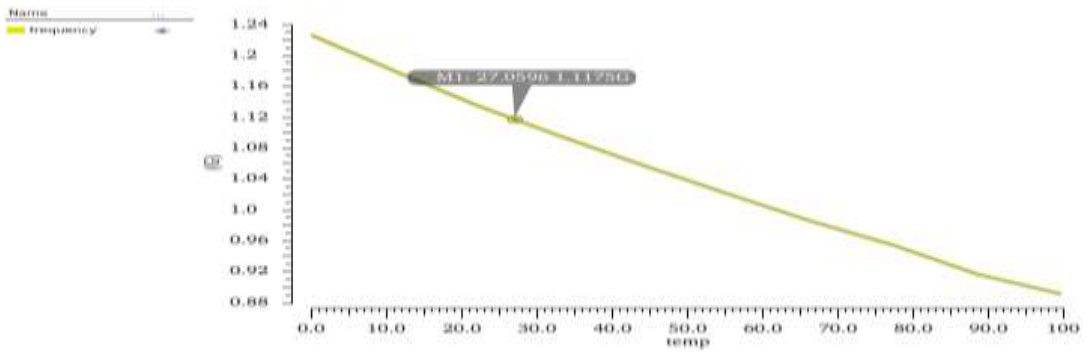

Figure15: Frequency vs Temperature in CSVCO

Figure15 gives the plot of frequency changes with respect to temperature. Here as the circuit is exposed to higher temperature the frequency is somewhat decreasing.

4.11 Corner Analysis for the current starved VCO

Table 5. Process Corner Analysis of CSVCO

Parameters	NN	FF	FS	SF	SS
Dynamic power (µW)	18.91	24.75	20.01	17.28	13.8
Static Power (pW)	33.28	226.3	73.99	18.67	10.85
Total power (µW)	18.91	24.76	20.01	17.28	13.8
Frequency (GHz)	1.12	1.482	1.206	1.007	.8036

Corner analysis is done for the current starved VCO is shown in table5.

4.12 Monte Carlo Analysis for CSVCO

Monte Carlo simulation is performed for total power and frequency in Cadence spectre at 45nm technology for N=200 samples and is shown in figure 16 and figure17. The mean and standard deviation is summarized in table 6.

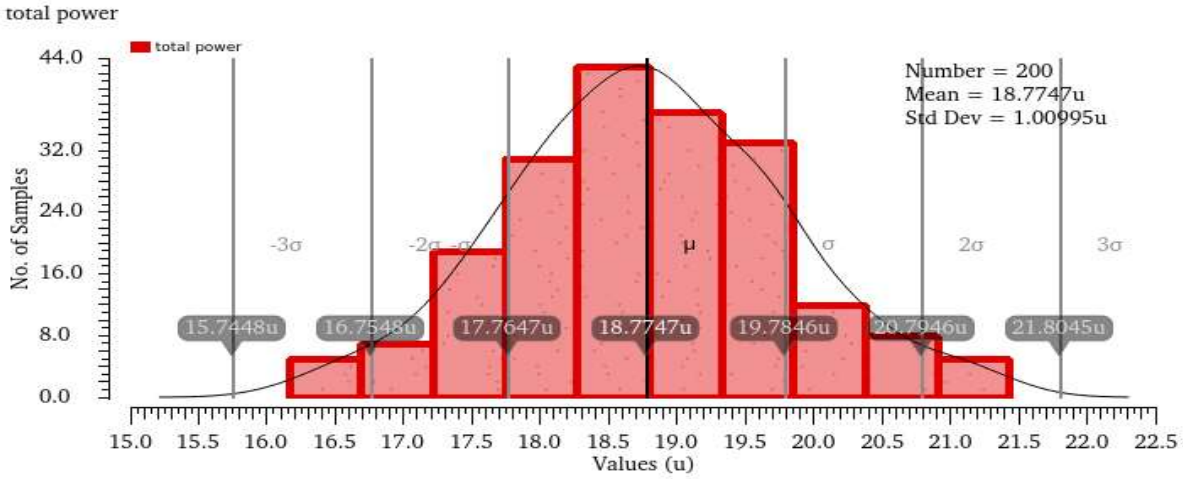

Figure 16: Monte Carlo Simulation result for total power (N=200)

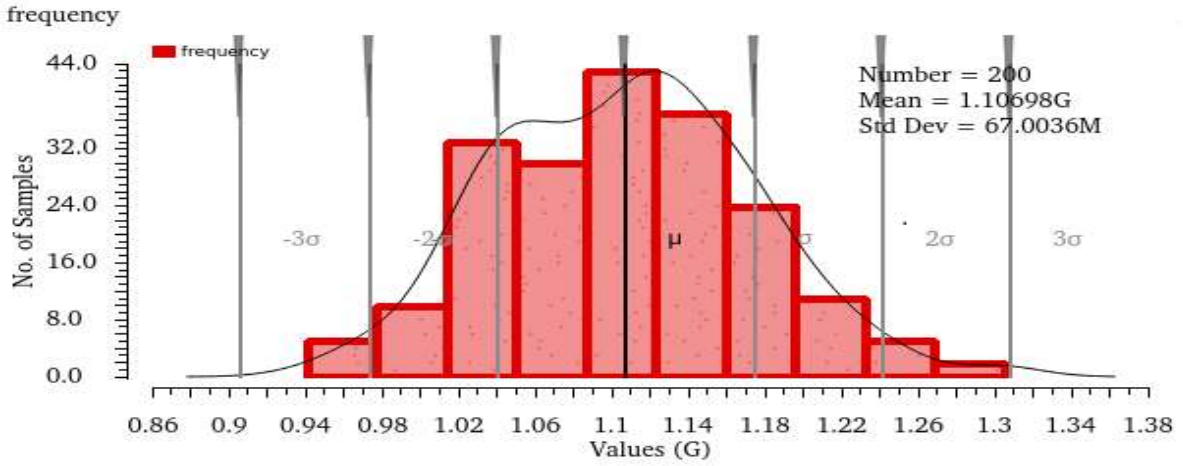

Figure 17: Monte Carlo Simulation result for frequency (N=200)

Table 6. Mean and standard deviation for frequency and total power using Monte Carlo

Parameter	Mean	Standard deviation(σ)
Frequency	1.107 GHz	67 MHz
Total power	18.77 µW	1.01 µW

4.13 Layout of the current starved VCO

The current starved VCO layout is designed in 45 nm technology with supply voltage of 1V and layout area of the circuit shown in figure 18 is 44.834µm^2.

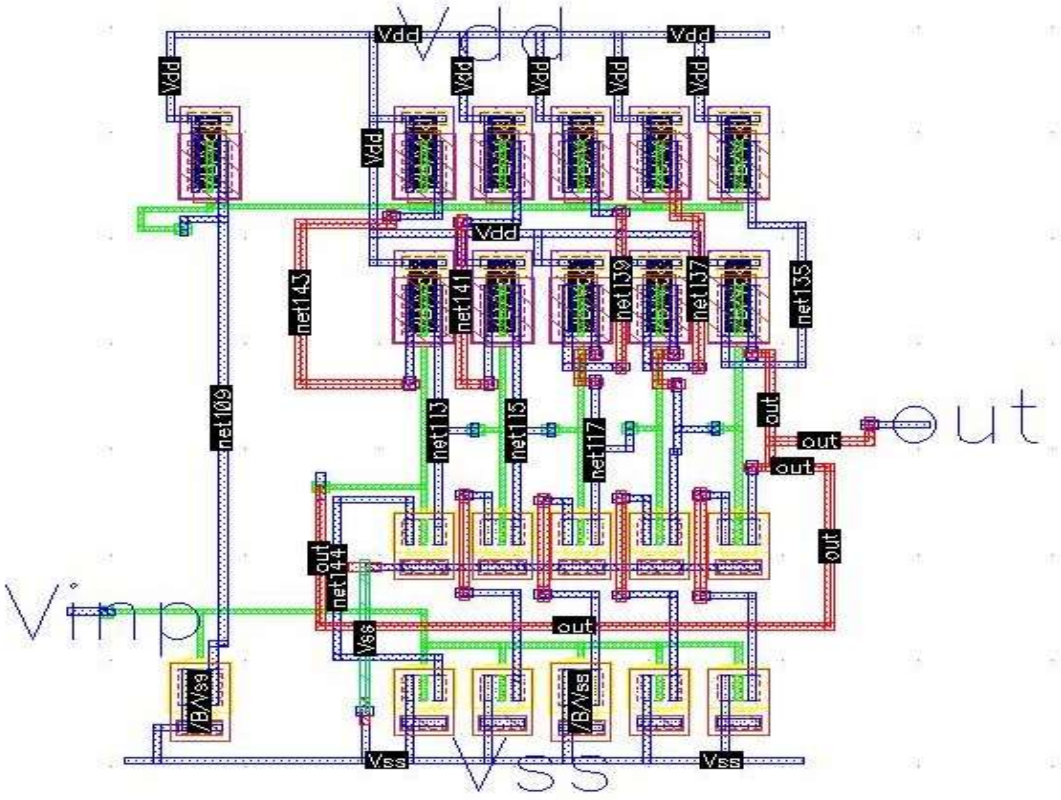

Figure18: Layout of the CSVCO

4.14 Performance comparison between different VCOs:

Table 7. Performance comparison between different VCOs

Parameter	IEICE [16]	DTIS [17]	JSSC [18]	This work
Supply Voltage	1.1	1	.6	1V
Oscillation frequency (GHz)	1.38	.450	.480	1.12
Total Power (µW)	1110	309	78	18.91
Number of transistors	11	NA	>32	22
Structure	Ring	Ring	Ring	Ring

The comparison of the CSVCO with the previous works are shown in Table 7. The previous work has effective oscillation frequency but with the high power consumption, lower area, and less tuning range, which is more unfit to the latest high-speed circuits. The benefit of the presented current starved VCO has high frequency with low power consumption. The circuit operates at a frequency of 1O MHz and supply voltage of 1V when compared to previous works observed that the circuit have low power dissipation of 18.91µW.

5. Conclusion

In this paper, a novel PFD is designed, charge pump and current starved VCO also presented. All these circuits are simulated using Cadence Virtuoso V6.1.7 gpdk 45nm CMOS technology with supply voltage 1V. The performance comparisons between various designs of PFDs are shown in table 3 and found out that proposed design achieves lowest power of 138 nW with significant operating frequency. This work also presented the design of charge pump which consumes power of 79.09µW. Furthermore, CSVCO is also designed at the operating frequency of 10 MHz with Vctrl=1V to give output oscillation frequency of 1.119GHz and total power of 18.91µW which is lesser. The performance comparisons between various designs of VCOs is shown in table 6 and found out that CSVCO consumes lower power than other designs. Corner analysis and Monte carlo analysis are successfully performed for the proposed PFD and CSVCO. These blocks are critical blocks and are used in applications like clock generation clock recovery, PLL.

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