reference crystal [6]. Introduction of multiple conversion levels can help in achieving wide measurement range at low resolution. This design involved multi-level conversion. The approach saw the use of differential delay cell for improving time resolution [7]. Adding and subtracting input signals has also been proposed in time domain signal processing. The design involved a time register for performing mathematical calculations with time signal [8]. Delay line TDC was used for high speed and clock was used to synchronize the pipeline stages. The sub-picosecond TDCs are widely used currently. Proceeding a step further to these designs, a novel TDC design proposed lately which computed difference between two consecutive delay time and used that information to generate digital code [9]. However, all these TDC designs had a drawback of high-power consumption.

Analog input voltage to time conversion in time-based ADCs is performed by Voltage to Time Converters, also known as VTCs. A number of VTC designs have been proposed till date as discussed ahead. In [10], VTC circuit is proposed to operate at 5 GS/s. However, the circuit consumes high power of 3.6 MW and has a small input dynamic range. In [11], a VTC circuit is proposed at which the input signal is compared with a voltage ramp. Although this design in Reference consumes low power, its operation is limited to small sampling frequency. In [12], a VTC is proposed that consists of a track and hold circuit, level shifter and a pulse shape restorer which improves the linearity of the VTC. However, this design suffers from high power consumption. Takauji proposed a current starved inverter made up of dual stage structure which improved the overall dynamic range. Yi too proposed a folding architecture based VTC design for implementing TBADC [13]. However, both these circuits consumed high power.

Osheroff presented a current mirror structure to achieve high linearity and high speed but had disadvantage of high-power consumption. Jia proposed a VTC circuit based on Current starved Inverter which employed folded structure [14]. Linearity of the circuit was improved but the power consumption rose up. In reference [15], a modified VTC is presented to increment linearity but the input dynamic range is limited to 400 mV along with the disadvantage of high power consumption. A digital time-based ADC is proposed to reduce the chip area but still the power consumption remained relatively high [16]. All these circuits had a common drawback of high-power consumption. The objective of this paper is to design a low power, high resolution time to digital converter along with proposing a novel voltage to time converter circuit design equipped with low propagation delay and high energy efficiency.

2. Time to Digital Converter Circuit

This section elaborates about the first circuit concerned with Time based ADCs, that is Time to Digital Converters. Vernier time to digital converter (VTDC) architecture has been considered for this work. The propagation delay $\boldsymbol{\tau}$ of a single delay element could be expressed as

$$\tau = \mathrm{C} * R \tag{1}$$

where:
C = load capacitance
R = resistance offered by circuit.
Resistance R can be elaborated by equation 2

$$R = V/I \tag{2}$$

where:
V = input voltage,
I = output current.