

Implementation of Modified folded Cascode OTA in Different Biasings Voltages

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Abstract: This paper presents an optimized methodology to modified folded Cascode operational trans conductance amplifier (OTA) design. The design is done in different regions of operation, weak inversion, strong inversion and moderate inversion using the gm/ID methodology in order to optimize MOS transistor sizing. This new family of OTA designs is suitable for biomedical and healthcare circuits and systems, due to the high energy-efficiency, improved gain and low level of noise contribution, when compared to the state-of-the-art in this field. In this paper, two fully-differential implementations are presented, a first one with a double CMOS branch biased by two pairs of voltage-combiners structures in both NMOS and PMOS configurations, and a second one with folded voltage-combiners specifically targeting low voltage applications. The folded voltage-combiners biased OTA is able to operate correctly under a voltage supply down to 0.7 V with proper DC biasing. The simulation is performed in HSPICE Synopsys Tool and compared with existing designs.

Index Terms – CMOS IC design, Folded Cascode OTA, gm/ID methodology, optimization.

1. INTRODUCTION

The development of wearable devices, particularly in the biomedical and healthcare field of applications, has grown much especially during the last two decades [1]. The sensors used in this field have special design and development restraints: the portability, the size and weight, the longevity, ergonomics and the power consumption in parallel with the energy-efficiency are among the most important aspects to take in consideration [2]. The devices must have small form factor and active area with low power consumption, enabling comfortable, unobtrusive and long-time monitoring, hence, suitable for daily use. Sensing amplifiers usually dominate the power and the noise of the recording frontend, therefore significant research activity has been focused on designing this block, taking into consideration the need for high gain and high energy-efficiency, with proposals of new strategies to overcome the challenges of modern CMOS technologies.

Particularly, the design of operational trans-conductance amplifiers (OTAs) in modern CMOS technologies, face now additional and special design challenges. Among these, it is perhaps the most important tradeoff to be considered, which opposes gain improvement techniques in a way that complies with a high energy-efficiency demand, under low biasing voltages and, furthermore, with a low noise impact. In fact, it is well known that the intrinsic gain (gm/g_{ds}) of CMOS technologies is suffering a considerable decrease [3,4] to an estimate value smaller than 20 dB, i.e., 10 V/V, while the variability of the intrinsic gain may be in the range of 10 dB, predominantly below standard 65 nm technological nodes. Therefore, new strategies must be proposed. On one hand, the implementation of massive cascode topologies are becoming unbearable due to the decrease of voltage supply values, i.e., stacking of transistors is becoming an important

issue. Inverter based cascaded designs are good choices if a high gain is desired, due to the ability of easily cascading several inverter stages in one amplification block. On the other hand, it is hard to build up closed-loop stable inverter based OTAs with low active-area, in a way that is free from the impact of mismatch and process imperfections, as well as the impact of corner conditions [5–7]. In this context, the usage of optimization algorithms in order to ensure the correct symmetry of this type of circuits and, in parallel, step up the advantages in terms of gain, speed and occupied active-area is completely justified. Furthermore, common performance tradeoffs in the design of single-stage amplifiers involve: high gain as opposed to high bandwidth, high gain as opposed to high energy-efficiency, high gain as opposed to reduced noise impact, reduced current consumption as opposed to high gain-bandwidth product, reduced current consumption as opposed to reduced noise impact, and high gain as opposed to reduced active-area of complete circuitry.

2. METHODOLOGY

A. Existing System

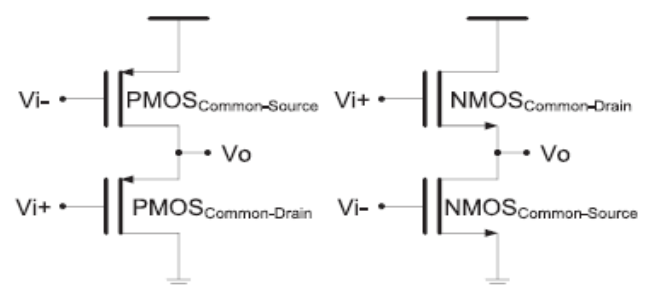


Fig. 1. Standard VCs: a) PMOS based; b) NMOS based

i) Inverter-based OTA biased by standard VCs

This paper presents a new family of inverter-based OTAs biased by voltage-combiners for gain and energy-efficiency improvement. This family encompasses a standard and a folded configuration. In the first case, i.e., the standard configuration, the biasing of the proposed inverter-based OTA is carried out by two pairs of cross-coupled PMOS and NMOS voltage-combiners. In the second case, i.e., in the folded configuration, the biasing is carried out also by two pairs of voltage combiners, yet in a folded configuration biased in current, for proper DC point in lower voltages, e.g., supplies below 1 V.

The schematic of a voltage-combiner in its standard configuration is shown in Fig. 1, for both PMOS and NMOS flavors. A mixture of two common-drain (CD) devices and two common source (CS) devices have a frequency-response similar to that of a first order low-pass filter [9].

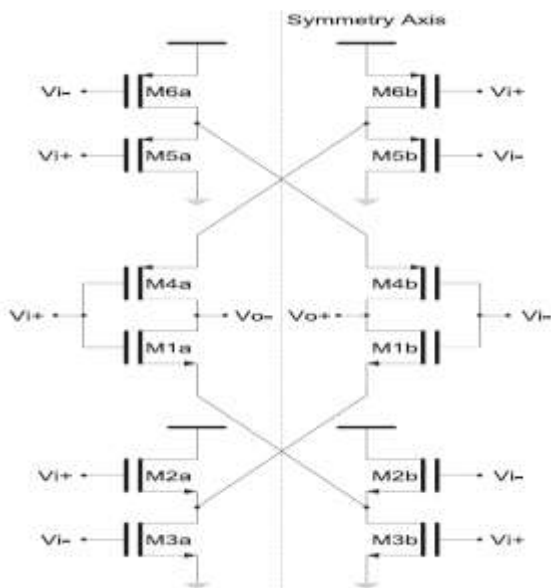


Fig. 2. Inverter-based OTA biased by standard VCs.

ii) Inverter-based OTA biased by Folded VCs

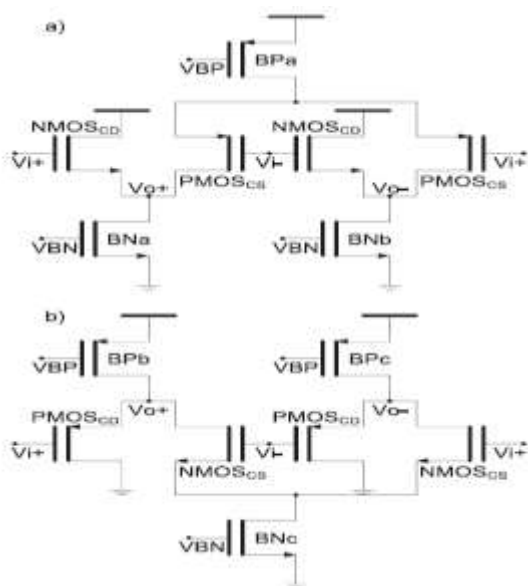


Fig. 3. Folded VCs: a) PMOS based; b) NMOS based.

The appropriate response to voltage supplies below 1 V relies on a topology in which the CD and CS devices are folded and are, furthermore, biased by current sources in a fully-differential configuration. The corresponding circuit schematic is shown in Fig. 3, where a doublet of folded voltage-combiners are designed to operate with a nominal supply spanning from 1.2 V down to 0.7 V without stacking issues, i.e., maintaining proper DC biasing. Furthermore, an implementation using low-voltage devices and the intrinsic biasing strategy of the circuit allow for a low current draining with operating point establishment, which otherwise would not be possible for lower supply voltages, e.g., below 1.8 V, using the standard VC approach. The circuit in Fig. 4 employs two PMOS devices in a CS configuration and two folded NMOS devices in a CD configuration, combined with differential input and output. This structure is biased in current by the top and bottom current sources [9]. The gain of the fully-differential folded VC circuit is given by (6), neglecting the body-effect.

The circuit schematic of the proposed folded VC biased CMOS inverter-based OTA is shown in Fig. 4. This circuit is compounded by two folded voltage-combiners structures which bias two inverter branches for further gain, as given in (11), and GBW enhancement. Manual design procedure follows the standard approach: establishment of a proper DC operating point (definition of the overdrive voltages and saturation margins); DC current budget in all branches is calculated.

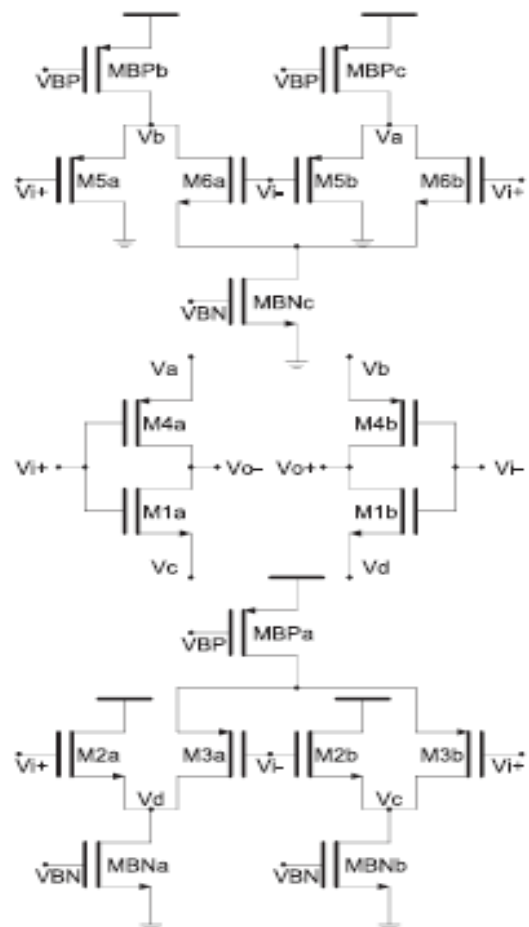


Fig. 4. Inverter-based OTA biased by folded VCs.

iii) **Folded Cascode OTA**

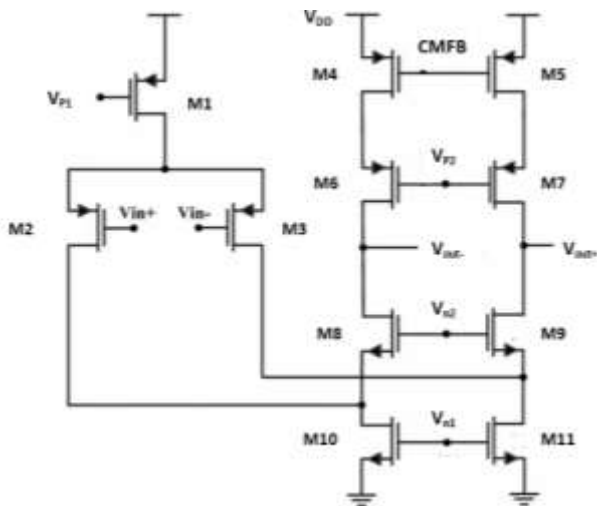


Fig.5. Folded Cascode OTA

The folded cascode OTA shown in fig.5 is folded first stage in PMOS based pull up network for better frequency response and good gain capable of operating at lower potentials of 1.2V, 1V and 0.7V. The second stage is similar to Wilson current mirror which the maximum output voltage is set lower than $V_{DD} + V_T + 2V_{ds,sat}$, so that the output voltage is restored to a minimum fall to $+2V_{ds,sat}$. The current that flows through M_1 , M_{10} and M_{11} is $2I_{SS}$ whereas the current through the transistors M_4 and M_5 is I_{SS} . With a proper bias supply for V_{n1} , V_{n2} , V_{p1} , V_{p2} and V_{CMFB} we get the required improvement in output potential and frequency response.

B. Proposed System

Modified Folded Cascode OTA

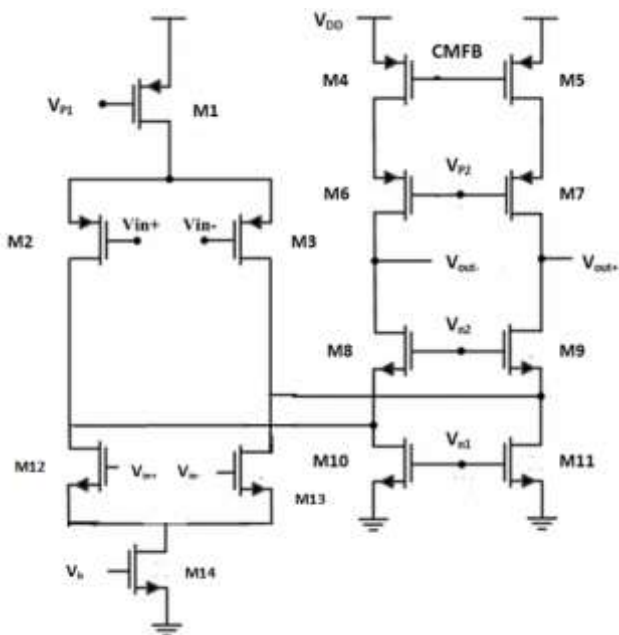


Fig.6. Modified Folded Cascode OTA

The modified folded cascode OTA aims improving the transconductance and the DC gain along with AC gain of the OTA. The modification is done in first stage with a NMOS based folding added to folded cascode OTA as

shown in fig.6. But the tail transistor M_{14} is biased by V_b rather than V_{n1} or V_{n2} . Hence the current through the transistor M_{14} is $2I_b$ and through the transistors M_{10} and M_{11} will be now I_b . The transconductance improves as V_{in} is used to drive M_{12} and M_{13} yielding twice the value of that of folded cascode OTA resulting better gain.

For the above designed circuits the common mode feedback potential is extracted from the circuit shown in fig.8.

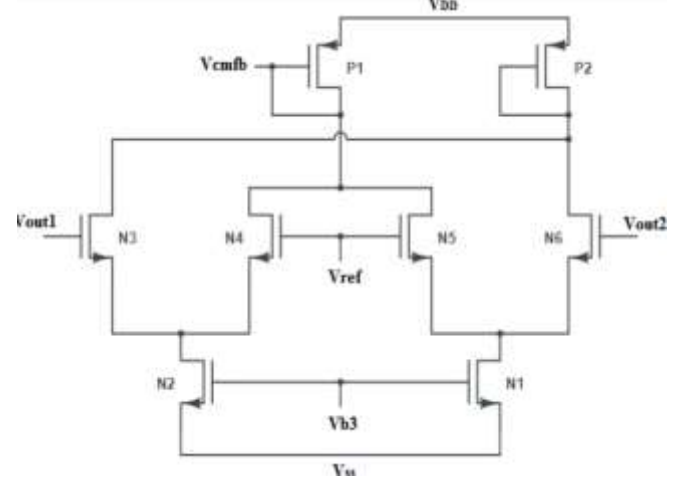


Fig.7. Common Mode Feedback Circuit

The V_{CMFB} is extracted from the V_{out+} and V_{out-} as V_{out1} and V_{out2} respectively connected in differential configuration. But still this circuit requires V_{ref} and V_{b3} for biasing the transistor sets $N_4 - N_5$ and $N_1 - N_2$.

The Common Mode Feedback circuit performs three operations i.e., it senses the common mode outputs of the fully differential OTA then compares the result with a reference voltage, normally the reference voltage (V_{ref}) is equal to half of the supply voltage, for \pm supply voltage the reference voltage should be zero; and then returns the error to the amplifiers bias network (VCMC) using negative feedback to set the common mode (CM) output value as shown in fig.7.

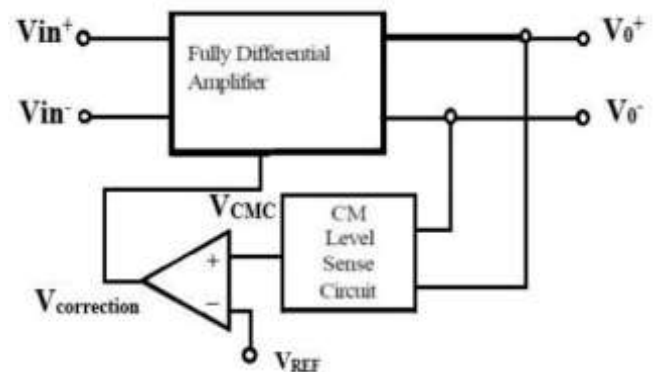


Fig.8. The basic block diagram of common mode feedback circuit

Thus, the OTA characteristics are enhanced by using CMOS inverter based Folded Cascode OTA. Also the design is done in different regions of operation i.e., weak inversion, strong inversion and moderate inversion using the g_m/ID methodology in order to optimize MOS transistor sizing. The basic block diagram of common mode feedback circuit Shown in fig.8.

The designs are modeled using SPICE Language and simulated HSPICE tool. The results developed are tabulated in tables I and II.

Table I: Comparison Table (Power in W)

Methods	OTA	0.7V	1V	1.2V
Existing Methods	Standard VCs (PMOS)	0.39×10^{-6}	1.2×10^{-6}	2.1×10^{-6}
	Standard VCs (NMOS)	9.18×10^{-15}	1.9×10^{-14}	2.7×10^{-14}
	Folded VCs (PMOS)	5.14×10^{-6}	14.2×10^{-6}	23.6×10^{-6}
	Folded VCs (NMOS)	4.7×10^{-6}	11.05×10^{-6}	17.43×10^{-6}
	Inverter based OTA biased by Folded VCs	9.81×10^{-6}	27.7×10^{-6}	44.8×10^{-6}
	Folded Cascode OTA	1.1×10^{-6}	2.9×10^{-6}	6.1×10^{-6}
Proposed Method	Modified Folded Cascode OTA	2.01×10^{-6}	5.8×10^{-6}	9.6×10^{-6}

From table I, the proposed method shows an improvement as the supply voltage reduces from 1.2V to 1V and to 0.7V with an improvement of 40.19% and 65.26% respectively.

Table II: Comparison Table (Delay in ns)

Methods	OTA	0.7V	1V	1.2V
Existing Methods	Standard VCs (PMOS)	10.028	4.5177	14.783
	Standard VCs (NMOS)	10.014	10.034	10.038
	Folded VCs (PMOS)	48.909	40.035	40.017
	Folded VCs (NMOS)	7.090	0.0693	0.0081
	Inverter based OTA biased by Folded VCs	82091.0	6131.2	326.29
	Folded Cascode OTA	5473.4	20.020	5324.6
Proposed Method	Modified Folded Cascode OTA	19.743	20.048	20.009

From table II, the proposed method shows an improvement as the supply voltage reduces from 1.2V to 1V and to 0.7V with an improvement of -0.19% and 1.52% respectively.

4. COMPARISON OF RESULTS

After discussing the different parameters of OTA design we can evaluate our study toward other works. The performance of the Modified folded cascode OTA from this work has been compared to Existing methods like folded cascode OTA. This comparison is given in table I in terms of Power in watts and in table II in terms if delay in ns. It is clearly seen that with modified folded cascode OTA architecture, we reach low power low delay in the biasing voltage 0.7V.

Consequently, the synthesis of high-performance analog integrated circuits constitutes a complex activity requiring the command of many concepts. As a result, the analog designer remains a rare and highly-valued engineer worldwide.

This contribution presents the strategy design of Modified folded cascode OTA in the biasing voltages such as 0.7V, 1V and 1.2V. We estimate that gm/ID methodology is well adopted for sizing in different function modes to reach extremely performances offered by a given technology.

Future work would involve the exploitation of these results on folded cascode OTA for low consumption and wide band applications to use it in wide band analog-to-digital converters.

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