Yield improvement in SMT process by adjusting input process parameter

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Abstract : Mass manufacturing of Electronics equipment has resulted change in process. Earlier most of the components were used to be through hole mounted. Presently components are mounted through machines. The process is known as Surface Mounted Technology (SMT). In SMT process, input parameters need to be accurate to get defect free output. Process input data need to be tailormade as per requirement. Once process data is established, automatically throughput will be improved.

Key words : SMT, Pcb, FTP, AOI.

1. Introduction:

Presently SMT technology is extensively used in Electronics equipment manufacturing. Automization of through hole process is very difficult[1]. Due to change in shape of component, the process for manufacturing is amenable to automation. The yield of SMT process depends upon setting of input parameter[2]. Once desired input parameter is established, through put will be increased automatically.

The power amplifier Pcb which is under discussion is used for Jamming purpose of mobile network. The pcb has three section:

1. Supply section : It converts 26 Volts supply into 5V output.
2. RF section : It has three stage amplifier (Pre-driver, Driver and Final amplifier). This section is primarily responsible for amplification of RF signals which is coming from synthesizer pcb.
3. Control section : It is primarily responsible for measurement of reverse and forward power of amplifier signal which is coming from final amplifier. The Pcb is shown in Fig 1.

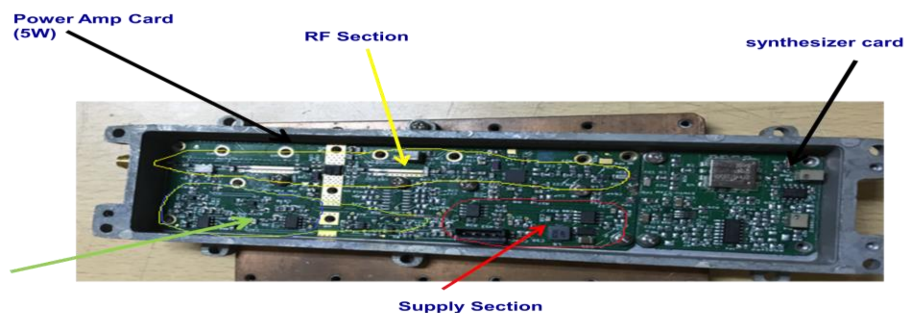


Fig 1: Power Amplifier Pcb

2. **Research Problem:**

As per production schedule power amplifier pcb were needed to be assembled for qty 7000 nos. within short period of time. It has been decided to assemble a pilot batch of small qty of pcb and analyse the results[3]. Based on analysis, input process parameters will be optimized to get defect free output. The manufacturing process diagram of Pcb manufacturing is shown in Fig 2.

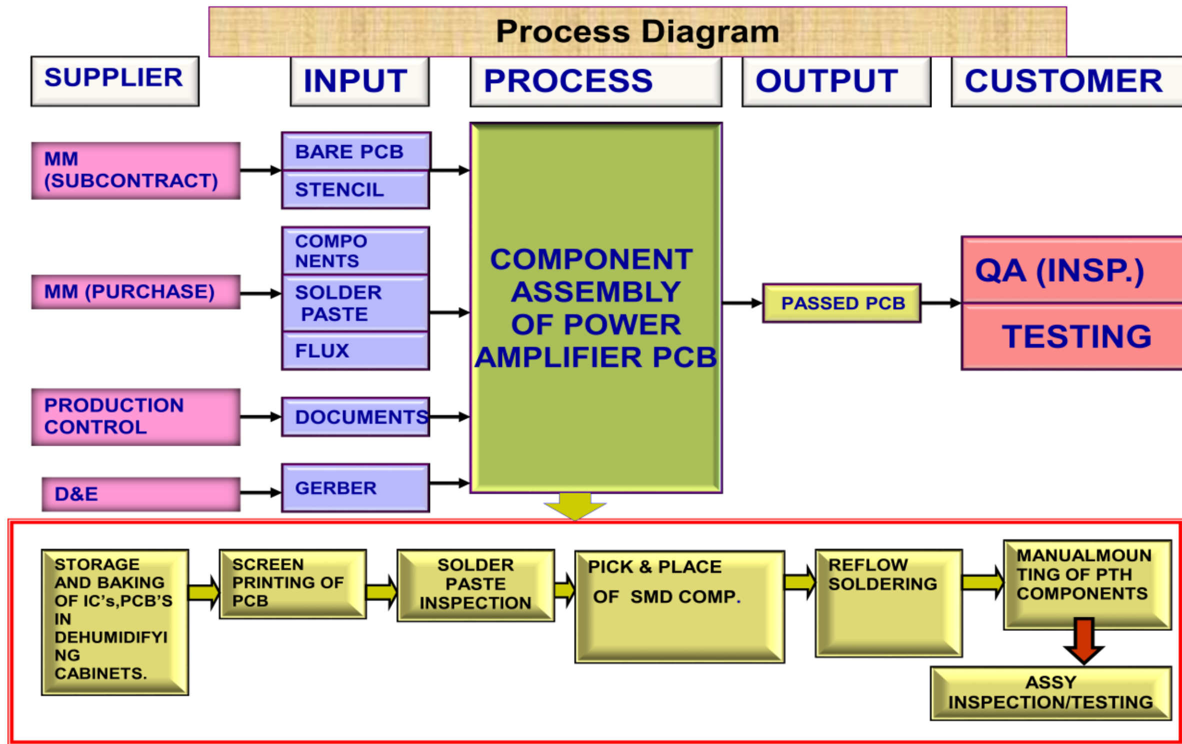


Fig 2: Process Diagram

The process mapping diagram is shown in Fig 3.

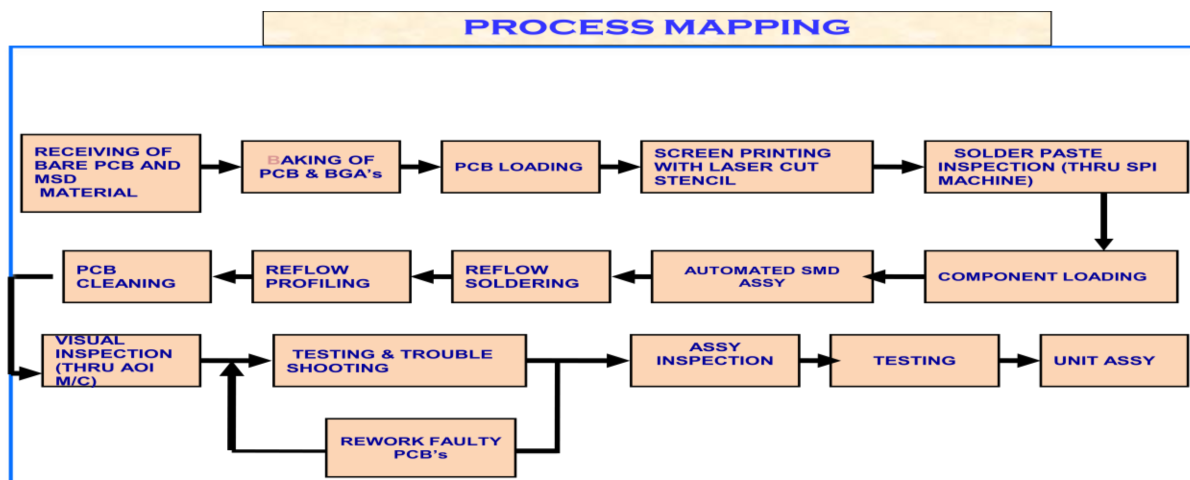


Fig 3: Process Mapping

Initial batch of 500 pcbs were assembled. Soldering joints were inspected for all 500 assembled pcbs through Automatic Optical Inspection (AOI) machine[4]. Defective solder joints were observed in some of the capicitors and few Ics. These defective joints were rectified by manual soldering and Pcbs were offered to QC and Testing[5].

Based on Testing feedback, Pcb defects were tabulated. Pcb defect data is shown in Fig 4.

MEASUREMENT OF DATA AT TESTING LEVEL

However still 619 soldering defects were observed at Testing Stage in 182 defective pcbs.

Total PCB's Offered	= 500 nos.
Total defectives	= 182 nos.
No. of defects in PCB's	= 619 nos.

Fig 4: Pcb defect data

Further to that individual components defect data was prepared which is shown in Fig 5.

LIST OF DEFECTS IN POWER AMPLIFIER

500 NOS.OF POWER AMPLIFIER PCBs INSPECTED / TESTED THOROUGHLY AND FOLLOWING TYPES OF DEFECTs FOUND AT TESTING LEVEL

TYPE OF PACKAGE	TYPE OF DEFECT	UNIT	OPP/PCB	TOTAL OP.	DEFECTS
CAPs,ICs,CONNCTR	SHORTING	500	146	73000	170
ICs, CAPs	Dry solder	500	409	204500	347
Others	Others	500	Not counted	Not Counted	102
Total		500	--	--	619

Total Opportunities = 277500

Total defects = 517 focused to resolve.

Other 102 defects came because of multiple reasons mainly because of operator's negligence. Hence, these were not considered significant.

Fig 5: List of Defects

It has been observed that first time pass percentage of pcb was 63.60 %, which is not satisfactory. It was decided to analyse the cause of failure so the input parameter can be modified accordingly to get maximum defect free pcb at testing stage[6].

3. Analysis:

The failure data was collated. To have in-depth understanding of process Cause & Effects diagram was prepared[7]. The diagram is shown in Fig 6.

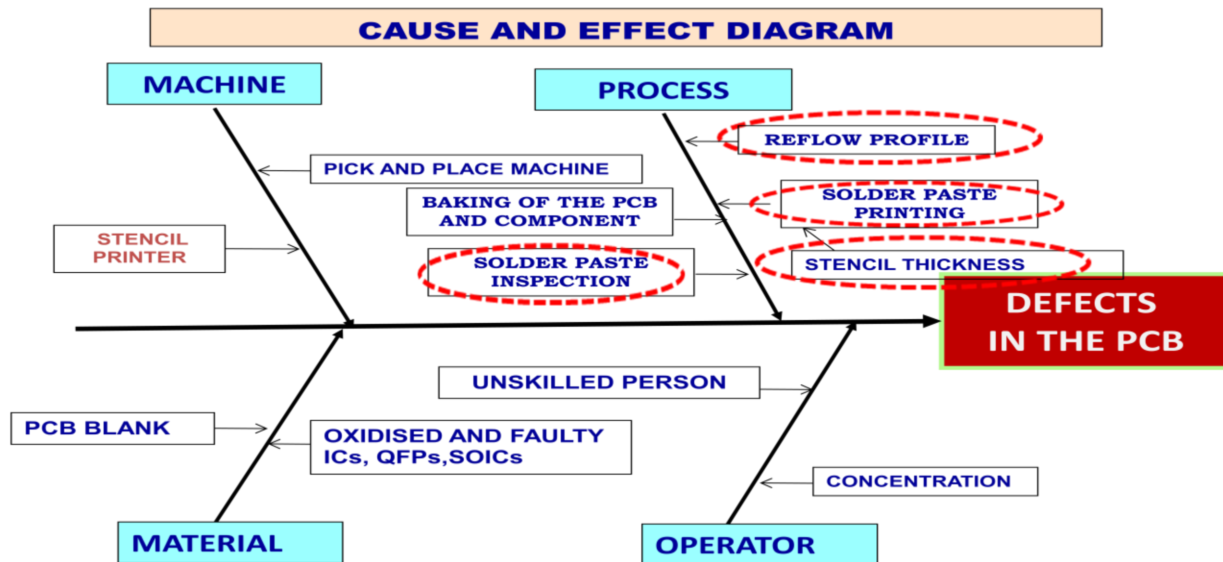


Fig 6: Cause & Effect Diagram

Some of the probable problem areas were highlighted. They are listed as:

1. Solder Paste Inspection
2. Reflow Profile.
3. Solder Paste Printing.
4. Stencil Thickness.

Following defects were observed and subsequently they were analysed:

a. Dry Solder of U2 and U5 ICs: The center aperture of stencil screen of U4 and U5 ICs is having 80% opening of area (as per IPC 752A). Dry solder was observed during inspection of these areas[8].
b. Shorting observed among there parallel capacitors C45, C46 and C47 : Aperture opening for all SMD chip components (Package size 0603 and bigger) were 100% (as per IPC 7525A Standard). Shorting was found during soldering due to less masking (gap) on bare pcb. This has caused bridging among three parallel capacitors.
c. Less solder volume observed during solder paste inspection stage: In general it was observed that less deposition of solder on pcb after solder paste application. This was observed during solder

paste inspection stage. Deposition of solder paste depends upon thickness of stencil screen. As per IPC Standard, 4 mil foil thickness sheet is to be used[9].

d. Shorting of components other than C45, C46, C47 and dry solder components (other than U4 and U5): The pcb assembly was complex in nature. It comprises of different types of SMD packages (Rohs & non Rohs) and having fine pitch ICs, QFN devices etc. Reflow profile used for initial lot of Pcb manufacturing might not have chosen correctly which might have resulted into dry solder, shorting, bridging and component failure.

One of the reasons of component failure was excess temperature application at the reflow profile. Maximum temperature at which component can withstand is called peak temperature. During reflow soldering if a component receives temperature in excess of peak temperature then inner bonding of device breaks. That leads to failure of the component. During failure analysis it is observed that some of the ICs (U4,U5 and U6) failed, which might be happened due to application of excess temperature[10].

Peak temperature of some of the ICs is shown in Table 1.

Sl No.	Device	Peak Body Temperature
1.	U4	249.73
2.	U5	249.73
3.	U6	249.73

Table 1: Peak temperature of ICs.

4. Improvements:

Each type of defect was analysed thoroughly and proper root cause analysis was done. Reflow profile temperature is optimized by studying critical components data sheet. For each critical component maximum temperature can withstand by component without any functional damage was noted down. Optimum profile was obtained by adjusting temperature profile and conveyor speed. For other defects corrective measures were taken by doing proper root cause analysis. Changes in parameter are shown in Table 2.

Sr. No.	Constant factors	Earlier Process	Improvement Plan
C1	SOLDER PASTE PRINTING PROCESS	SOLDER PASTE PRINTING ON PCB WITH OLD STENCIL HAVING 80% OPENING IN CENTER APERTURE (U4&U5) & 100% OPENING FOR SMD CHIP	NEW STENCIL WAS MADE FROM SUPPLIER(M/s ASAHITEC) WITH 85% OPENING OF CENTER APERTURE (U4,U5) & PAD REDUCTION IN 3 SMD CHIPS ONLY 70% OPENING.

		ITEMS(C45,C46,C47).	
C2	STENCIL THICKNESS	OLD STENCIL WAS OF 4 MIL FOIL THICKNESS CAUSING LESS VOLUME ON CENTRE PADS OF ICs.	NEW STENCIL WAS MADE OF 5 MIL THICKNESS.
C3	SOLDER PASTE INSPECTION	IN OLD SPI PROGRAM 10-15 % TOLERANCE WAS GIVEN TO CHECK SOLDER PASTE HEIGHT,VOLUME ON PADS.	NEW SPI PROGRAM MADE ON SPI MACHINE WITH TIGHT TOLERANCES (5%) TO CHECK SOLDER PASTE VOLUME ON SMD PADS.

C4	REFLOW SOLDERING PROFILE	IN OLD REFLOW PROFILE PEAK ZONE TEMP WAS SET 270 270 265 265 CONVEYOR SPEED=60 CM/MIN PWI = 70% PEAK BODY TEMP ON THE IC BODY WITH OLD REFLOW PROFILE WAS U4 249.73 degree U5 249.73 degree U6 247.43 (HIGH PROBABILITY OF DEVICE FAILURE)	IN OLD REFLOW PROFILE PEAK ZONE TEMP WAS SET 265 265 260 260 CONVEYOR SPEED=56 CM/MIN PWI = 45% Note: LESS PWI BETTER THE PROCESS PEAK BODY TEMP ON THE IC BODY WITH NEW REFLOW PROFILE IS U4 237.83 degree U5 238.90 degree U6 241.05 degree (LESS PROBABILITY OF DEVICE FAILURE)

Table 2: Improvement Table

Improvements in defects are shown on Fig 7, Fig 8 and Fig 9.

IMPROVEMENT – MODIFICATION IN STENCIL THICKNESS AND APERTURE

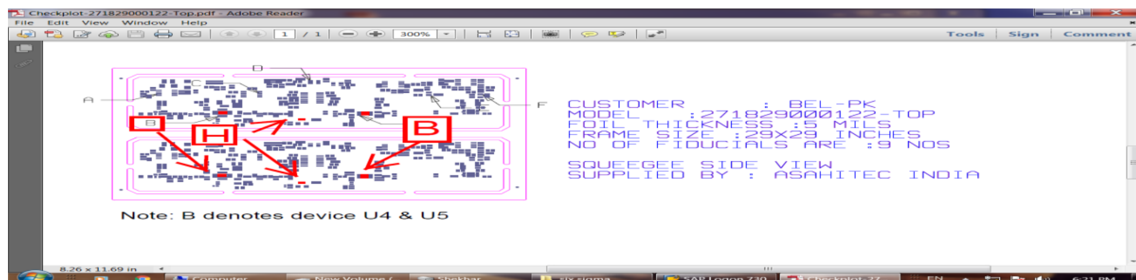


Fig 7 : Stencil thickness change and increase in center aperture for ICs.

IMPROVEMENT – MODIFICATION IN STENCIL APERTURES

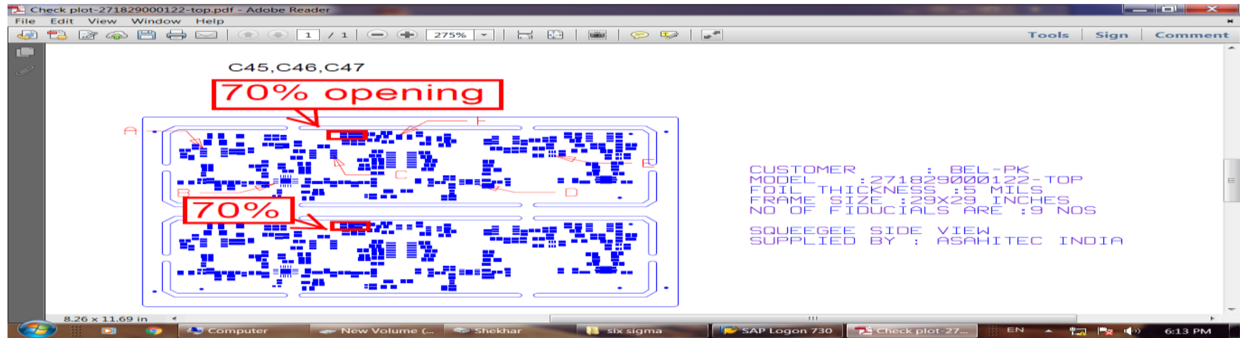


Fig 8: Decrease in Stencil apertures for capacitors

IMPROVEMENT – SOLDER PASTE ON CENTER PAD U4,U5 WITH NEW STENCIL

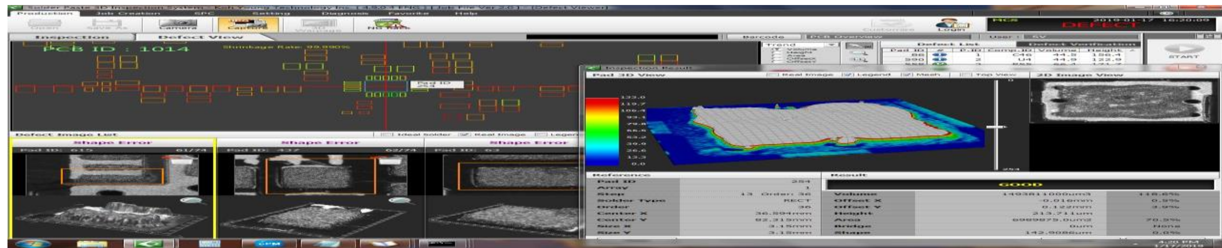


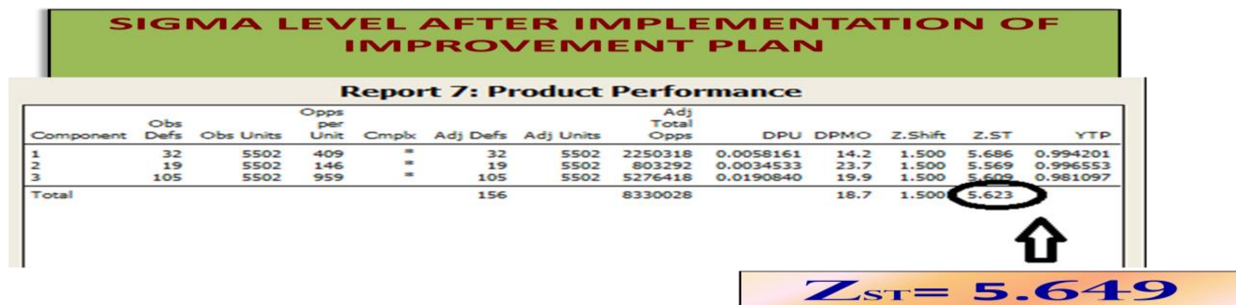
Fig 9: Increase in thickness of solder paste for centre pad opening of ICs

5. Results:

After carrying out all improvements qty 5502 nos pcbs were assembled and out of that 156 defects are observed. List of defects is shown in Table 3.

PCb assembled	5502
No of defects	156

Table 3: Defect list



SIGMA LEVEL AFTER IMPLEMENTATION OF IMPROVEMENT PLAN

Report 7: Product Performance

Component	Obs Defs	Obs Units	Opps per Unit	Cmplx	Adj Defs	Adj Units	Adj Total Opps	DPU	DPMO	Z.Shift	Z.ST	YTP
1	32	5502	409	*	32	5502	2250318	0.0058161	14.2	1.500	5.686	0.994201
2	19	5502	146	*	19	5502	803292	0.0034533	23.7	1.500	5.569	0.996553
3	105	5502	959	*	105	5502	5276418	0.0190840	19.9	1.500	5.609	0.981097
Total					156		8330028		18.7	1.500	5.623	

Z_{ST}= 5.649

Fig 10: Sigma level

After improvement was carried out, sigma level of the process was calculated as Zst = 5.649. calculation shown in Fig. 10.

Simillarly Chi square test was conducted. P value < .05, hence the improvent is significant. The Chi suare test is shown in Fig 11.

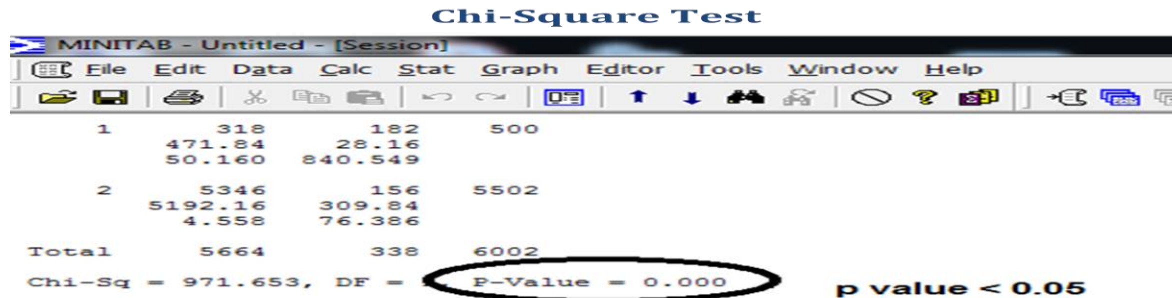


Fig 11: Chi square test result

First time pass data was calculated. Detail is shown in Fig 12. Pass time pass after improvement is 97.16%.

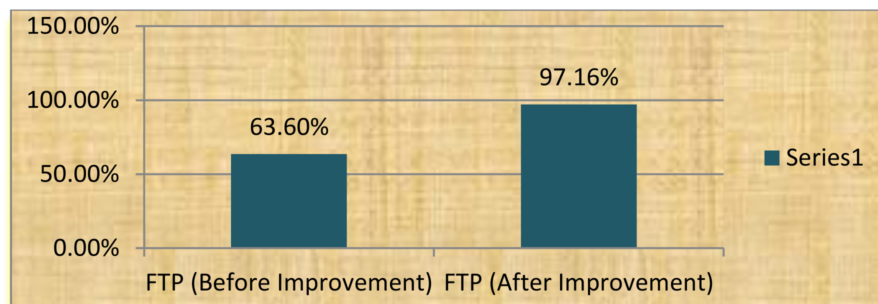


Fig 12: First time pass data.

6. Conclusion:

The following are the outcome:

1. There is drastic improvement in first time pass of the pcb from 63.60% to 97.16%.
2. The throughput is increased which resulted in lesser rework and thus project completion time is significantly reduced.
3. The reliability of the product is increased since lesser rework is done on the product.

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AUTHORS PROFILE

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Mr. Chandra Sekhar is presently working in Bharat Electronics Ltd, Panchkula. He is a Mechanical Engineer. He is working as manager in SMT assembly area. He has expertise on SMT processes and come out with various reflow soldering profile where soldering defects are negligible. He has done a quite number of six sigma projects.